LM5122 Wide-Input Synchronous Boost Controller With Multiple Phase Capability

1 Features

- Maximum Input Voltage: 65 V
- Minimum Input Voltage: 3 V (4.5 V for Start-Up)
- Output Voltage up to 100 V
- Bypass ($V_{OUT} = V_{IN}$) Operation
- 1.2-V Reference with ±1% Accuracy
- Free-Run and Synchronizable Switching to 1 MHz
- Peak-Current-Mode Control
- Robust 3-A Integrated Gate Drivers
- Adaptive Dead-Time Control
- Optional Diode-Emulation Mode
- Programmable Cycle-by-Cycle Current Limit
- Hiccup-Mode Overload Protection
- Programmable Line UVLO
- Programmable Soft Start
- Thermal Shutdown Protection
- Low Shutdown Quiescent Current: 9 μA
- Programmable Slope Compensation
- Programmable Skip-Cycle Mode Reduces Standby Power
- Allows External VCC Supply
- Inductor DCR Current Sensing Capability
- Multi-phase Capability
- Thermally Enhanced 20 or 24-Pin HTSSOP
- Create a Custom Design Using the LM5122 With the WEBENCH® Power Designer

2 Applications

- 12-V, 24-V, and 48-V Power Systems
- Automotive Start-Stop
- Audio Power Supply
- High-Current Boost Power Supply

3 Description

The LM5122 is a multi-phase capable synchronous boost controller intended for high-efficiency synchronous boost regulator applications. The control method is based upon peak-current-mode control. Current-mode control provides inherent line feed forward, cycle-by-cycle current limiting, and ease of loop compensation.

The switching frequency is programmable up to 1 MHz. Higher efficiency is achieved by two robust N-channel MOSFET gate drivers with adaptive dead-time control. A user-selectable diode-emulation mode also enables discontinuous-mode operation for improved efficiency at light load conditions.

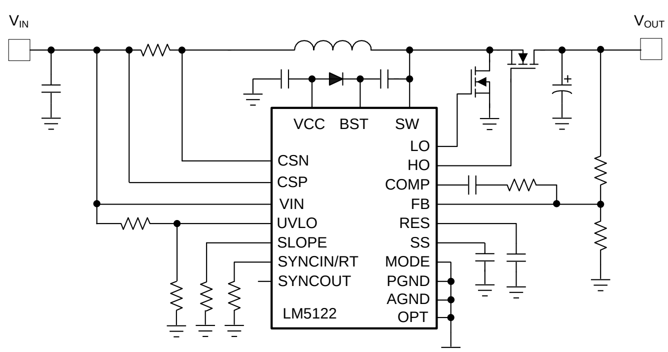
An internal charge pump allows 100% duty cycle for high-side synchronous switch (bypass operation). A 180° phase shifted clock output enables easy multi-phase interleaved configuration. Additional features include thermal shutdown, frequency synchronization, hiccup-mode current limit, and adjustable line undervoltage lockout.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5122	HTSSOP (20)	6.50 mm × 4.40 mm
LM5122Z	HTSSOP (24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from May 1, 2017 to June 9, 2017	Page
• Changed by splitting out the automotive datasheet from this commercial datasheet	1
• Added 24-pin HTTSOP package option	1
• Added links for WEBENCH	1
• Added 24-HTSSOP pin configuration	4
• Added 24-HTSSOP Functions	5
• Changed UVLO value	6
• Changed VCC value	6
• Changed one NC value	6
• Changed from outlet to contact	6
• Added LM5122Z part number	6
• Changed 20-HTSSOP Thermal Information and added 24-HTSSOP thermal values	7
• Added I_{CSP} –I_{CSN} (LM5122Z only) specs	9
• Added No load, 50% to 50% (LM5122Z only) specs	10
• Added 24-pin HTSSOP	14
• Added Negative to Positive conversion example	34

Changes from Revision F (May 2015) to Revision G	Page
• Added Automotive ESD feature	1
• Added paragraph and second equation	22
• Changed equation	22

Changes from Revision E (December 2014) to Revision F	Page
• Changed Handling Ratings to *ESD Ratings* and moved Storage temperature to *Absolute Max Ratings*	6
• Added Ohm symbol in *Current Sense Resistor* R_S equation 28	37
• Changed typo to reflect an Ohm symbol in *Current Sense Resistor* R_S equation 29	37

Changes from Revision D (September 2013) to Revision E	Page
• Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision C (August, 2013) to Revision D	Page
• Changed 5 kΩ to 20 kΩ	8
• Changed C_{COMP} to C_{HF}	42

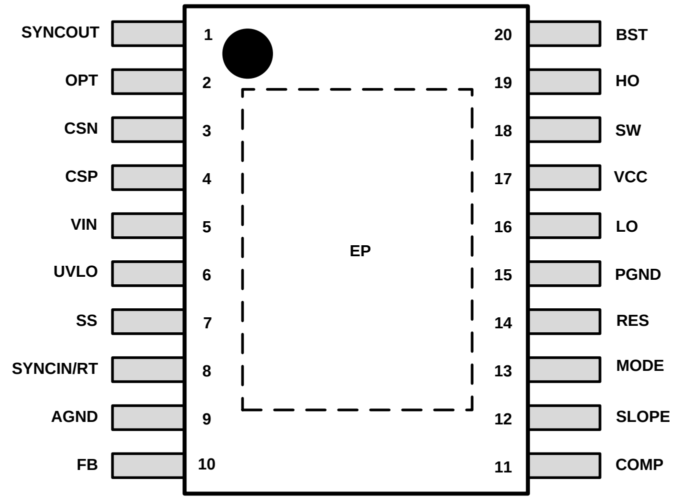
Changes from Revision B (May, 2013) to Revision C	Page
• Deleted Package Addendum	44

Changes from Revision A (May, 2013) to Revision B	Page
• Deleted Device Info table	5

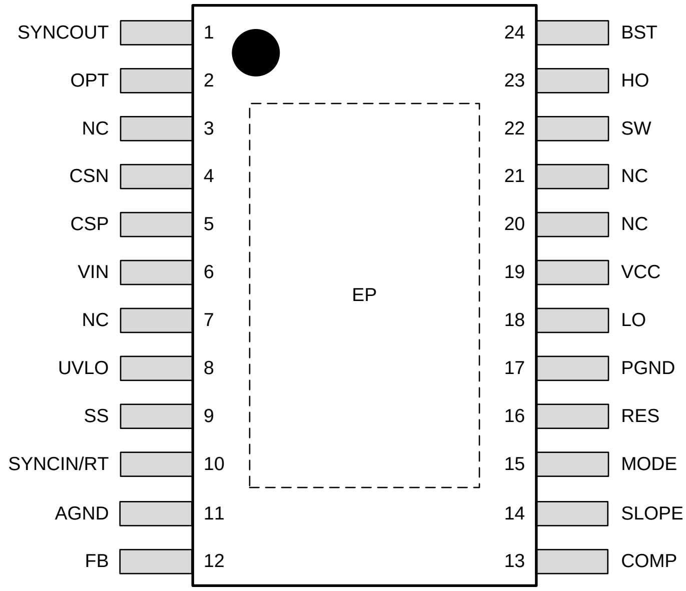
Changes from Original (March, 2013) to Revision A	Page
• Released full datasheet.	5

5 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP With Exposed Pad
Top View



PWP Package
24-Pin HTSSOP With Exposed Pad
Top View



Pin Functions

PIN			TYPE (1)	DESCRIPTION
NAME	24-Pin	20-Pin		
AGND	11	9	G	Analog ground connection. Return for the internal voltage reference and analog circuits.
BST	24	20	P	High-side driver supply for bootstrap gate drive. Connect to the cathode of the external bootstrap diode and to the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high-side N-channel MOSFET gate and should be placed as close to controller as possible. An internal BST charge pump supplies 200-µA current into bootstrap capacitor for bypass operation.
COMP	13	11	O	Output of the internal error amplifier. Connect the loop compensation network between this pin and the FB pin.
CSN	4	3	I	Inverting input of current sense amplifier. Connect to the negative-side of the current sense resistor.
CSP	5	4	I	Non-inverting input of current sense amplifier. Connect to the positive-side of the current sense resistor.
FB	12	10	I	Feedback. Inverting input of the internal error amplifier. A resistor divider from the output to this pin sets the output voltage level. The regulation threshold at the FB pin is 1.2 V. The controller is configured as slave mode if the FB pin voltage is above 2.7 V at initial power-on.
HO	23	19	O	High-side N-channel MOSFET gate drive output. Connect to the gate of the high-side synchronous N-channel MOSFET switch through a short, low inductance path.
LO	18	16	O	Low-side N-channel MOSFET gate drive output. Connect to the gate of the low-side N-channel MOSFET switch through a short, low inductance path.
MODE	15	13	I	Switching mode selection pin. 700-kΩ pullup and 100-kΩ pulldown resistor internal hold MODE pin to 0.15 V as a default. By adding external pullup or pulldown resistor, MODE pin voltage can be programmed. When MODE pin voltage is greater than 1.2-V diode emulation mode threshold, forced PWM mode is enabled, allowing current to flow in either direction through the high-side N-channel MOSFET switch. When MODE pin voltage is less than 1.2 V, the controller works in diode emulation mode. Skip cycle comparator is activated as a default. If MODE pin is grounded, the controller still operates in diode emulation mode, but the skip cycle comparator will not be triggered in normal operation, this enables pulse skipping operation at light load.
OPT	2	2	I	Clock synchronization selection pin. This pin also enables/disables SYNCOUT related with master/slave configuration. The OPT pin should not be left floating.
PGND	17	15	G	Power ground connection pin for low-side N-channel MOSFET gate driver. Connect directly to the source terminal of the low-side N-channel MOSFET switch.
RES	16	14	O	The restart timer pin for an external capacitor that configures hiccup mode off-time and restart delay during over load conditions. Connect directly to the AGND when hiccup mode operation is not required.
SLOPE	14	12	I	Slope compensation is programmed by a single resistor between SLOPE and the AGND.
SS	9	7	I	Soft-start programming pin. An external capacitor and an internal 10-µA current source set the ramp rate of the internal error amplifier reference during soft-start.
SW	22	18	I/O	Switching node of the boost regulator. Connect to the bootstrap capacitor, the source terminal of the high-side N-channel MOSFET switch and the drain terminal of the low-side N-channel MOSFET switch through short, low inductance paths.
SYNCIN/RT	10	8	I	The internal oscillator frequency is programmed by a single resistor between RT and the AGND. The internal oscillator can be synchronized to an external clock by applying a positive pulse signal into this SYNCIN pin. The recommended maximum internal oscillator frequency in master configuration is 2 MHz which leads to 1 MHz maximum switching frequency.
SYNCOUT	1	1	O	Clock output pin. SYNCOUT provides 180° shifted clock output for an interleaved operation. SYNCOUT pin can be left floating when it is not used. See *Slave Mode and SYNCOUT* section.

(1) G = Ground, I = Input, O = Output, P = Power

Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	24-Pin	20-Pin		
UVLO	8	6	I	Undervoltage lockout programming pin. If the UVLO pin is below 0.4 V, the regulator is in the shutdown mode with all functions disabled. If the UVLO pin voltage is greater than 0.4 V and below 1.2 V, the regulator is in standby mode with the VCC regulator operational and no switching at the HO and LO outputs. If the UVLO pin voltage is above 1.2 V, the start-up sequence begins. A 10-µA current source at UVLO pin is enabled when UVLO exceeds 1.2 V and flows through the external UVLO resistors to provide hysteresis. The UVLO pin should not be left floating.
VCC	19	17	P/O/I	VCC bias supply pin. Locally decouple to PGND using a low ESR/ESL capacitor located as close as possible to controller.
VIN	6	5	P/I	Supply voltage input source for the VCC regulator. Connect to input capacitor and source power supply connection with short, low impedance paths.
EP		EP	N/A	Exposed pad of the package. No internal electrical connections. Must be soldered to the large ground plane to reduce thermal resistance.
NC	3, 7, 20, 21	—		No electrical contact

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input	VIN, CSP, CSN	–0.3	75	V
	BST to SW, FB, MODE, UVLO, OPT, VCC[2]	–0.3	15	V
	SW	–5	105	V
	BST	–0.3	115	V
	SS, SLOPE, SYNCIN/RT	–0.3	7	V
	CSP to CSN, PGND	–0.3	0.3	V
Output[3]	HO to SW	–0.3	BST to SW + 0.3	V
	LO	–0.3	VCC + 0.3	V
	COMP, RES, SYNCOUT	–0.3	7	V
Thermal	Junction temperature	–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Unless otherwise specified, all voltages are referenced to AGND pin.
(2) See *Application and Implementation* when input supply voltage is less than the VCC voltage.
(3) All output pins are not specified to have an external voltage applied.

6.2 ESD Ratings: LM5122, LM5122Z

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per JESD22-A114 [1]	±2000	V
		Charged device model (CDM), per JESD22-C101 [2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input supply voltage(2)	VIN	4.5	65	V
Low-side driver bias voltage	VCC		14	V
High-side driver bias voltage	BST to SW	3.8	14	V
Current sense common mode range(2)	CSP, CSN	3	65	V
Switch node voltage	SW		100	V
Junction temperature, T_J		–40	125	°C

(1) Recommended Operating Conditions are conditions under which operation of the device is intended to be functional, but do not ensure specific performance limits.
(2) Minimum VIN operating voltage is always 4.5 V. The minimum input power supply voltage can be 3 V after start-up, assuming VIN voltage is supplied from an available external source.

6.4 Thermal Information

THERMAL METRIC		LM5122, LM5122Z		UNIT
		PWP		
		20 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36	32.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.1	15.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.8	7.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.7	7.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	1.1	°C/W

6.5 Electrical Characteristics

Unless otherwise specified, these specifications apply for –40°C ≤ T_J ≤ +125°C, V_{VIN} = 12 V, V_{VCC} = 8.3 V, R_T = 20 kΩ, no load on LO and HO. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN SUPPLY						
$I_{SHUTDOWN}$	VIN shutdown current	V_{UVLO} = 0 V		9	17	µA
I_{BIAS}	VIN operating current (exclude the current into RT resistor)	V_{UVLO} = 2 V, non-switching		4	5	mA
VCC REGULATOR						
$V_{CC(REG)}$	VCC regulation	No load	6.9	7.6	8.3	V
	VCC dropout (VIN to VCC)	V_{VIN} = 4.5 V, no external load			0.25	V
		V_{VIN} = 4.5 V, I_{VCC} = 25 mA		0.28	0.5	V
	VCC sourcing current limit	V_{VCC} = 0 V	50	62		mA
I_{VCC}	VCC operating current (exclude the current into RT resistor)	V_{VCC} = 8.3 V		3.5	5	mA
		V_{VCC} = 12 V		4.5	8	mA
	VCC undervoltage threshold	VCC rising, V_{VIN} = 4.5 V	3.9	4	4.1	V
		VCC falling, V_{VIN} = 4.5 V			3.7	V
	VCC undervoltage hysteresis			0.385		V
UNDERVOLTAGE LOCKOUT						
	UVLO threshold	UVLO rising	1.17	1.2	1.23	V
	UVLO hysteresis current	V_{UVLO} = 1.4 V	7	10	13	µA
	UVLO standby enable threshold	UVLO rising	0.3	0.4	0.5	V
	UVLO standby enable hysteresis			0.1	0.125	V

Electrical Characteristics (continued)

Unless otherwise specified, these specifications apply for –40°C ≤ T_J ≤ +125°C, V_{VIN} = 12 V, V_{VCC} = 8.3 V, R_T = 20 kΩ, no load on LO and HO. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MODE						
	Diode emulation mode threshold	MODE rising	1.2	1.24	1.28	V
	Diode emulation mode hysteresis			0.1		V
	Default MODE voltage		145	155	170	mV
	Default skip cycle threshold	COMP rising, measured at COMP		1.290		V
		COMP falling, measured at COMP		1.245		V
	Skip cycle hysteresis	Measured at COMP		40		mV
ERROR AMPLIFIER						
V_{REF}	FB reference voltage	Measured at FB, $V_{FB} = V_{COMP}$	1.188	1.2	1.212	V
	FB input bias current	$V_{FB} = V_{REF}$		5		nA
V_{OH}	COMP output high voltage	I_{SOURCE} = 2 mA, V_{VCC} = 4.5 V	2.75			V
		I_{SOURCE} = 2 mA, V_{VCC} = 12 V	3.4			V
V_{OL}	COMP output low voltage	I_{SINK} = 2 mA			0.25	V
A_{OL}	DC gain			80		dB
f_{BW}	Unity gain bandwidth			3		MHz
	Slave mode threshold	FB rising		2.7	3.4	V
OSCILLATOR						
f_{SW1}	Switching frequency 1	R_T = 20 kΩ	400	450	500	kHz
f_{SW2}	Switching frequency 2	R_T = 10 kΩ	775	875	975	kHz
	RT output voltage			1.2		V
	RT sync rising threshold	RT rising		2.5	2.9	V
	RT sync falling threshold	RT falling	1.6	2		V
	Minimum sync pulse width		100			ns
SYNCOUT						
	SYNCOUT high-state voltage	$I_{SYNCOUT}$ = –1 mA	3.3	4.3		V
	SYNCOUT low-state voltage	$I_{SYNCOUT}$ = 1 mA		0.15	0.25	V
OPT						
	Synchronization selection threshold	OPT rising	2	3	4	V
SLOPE COMPENSATION						
	SLOPE output voltage		1.17	1.2	1.23	V
V_{SLOPE}	Slope compensation amplitude	R_{SLOPE} = 20 kΩ, f_{SW} = 100 kHz, 50% duty cycle, T_J = –40°C to 125°C	1.375	1.65	1.925	V
		R_{SLOPE}= 20 kΩ, f_{SW}= 100 kHz, 50% duty cycle, T_J = 25°C	1.4	1.65	1.9	V
SOFT START						
$I_{SS\text{-}SOURCE}$	SS current source	V_{SS} = 0 V	7.5	10	12	µA
	SS discharge switch $R_{DS\text{-}ON}$			13		Ω
PWM COMPARATOR						
$t_{LO\text{-}OFF}$	Forced LO off-time	V_{VCC} = 5.5 V		330	400	ns
		V_{VCC} = 4.5 V		560	750	ns
$t_{ON\text{-}MIN}$	Minimum LO on-time	R_{SLOPE} = 20 kΩ		150		ns
		R_{SLOPE} = 200 kΩ		300		ns
	COMP to PWM voltage drop	T_J = –40°C to 125°C	0.95	1.1	1.25	V
		T_J = 25°C	1	1.1	1.2	V

Electrical Characteristics (continued)

Unless otherwise specified, these specifications apply for –40°C ≤ T_J ≤ +125°C, V_{VIN} = 12 V, V_{VCC} = 8.3 V, R_T = 20 kΩ, no load on LO and HO. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE / CYCLE-BY-CYCLE CURRENT LIMIT						
V_{CS-TH1}	Cycle-by-cycle current limit threshold	CSP to CSN, T_J = –40°C to 125°C	65.5	75	87.5	mV
		CSP to CSN, T_J = 25°C	67	75	86	mV
V_{CS-ZCD}	Zero cross detection threshold	CSP to CSN, rising		7		mV
		CSP to CSN, falling	0.5	6	12	mV
	Current sense amplifier gain			10		V/V
I_{CSP}	CSP input bias current			12		µA
I_{CSN}	CSN input bias current			11		µA
	Bias current matching	I_{CSP} – I_{CSN}	–1.75	1	3.75	µA
		I_{CSP} – I_{CSN} (LM5122Z only)	–2.5	1	8.75	
	CS to LO delay	Current sense / current limit delay		150		ns
HICCUP-MODE RESTART						
V_{RES}	Restart threshold	RES rising	1.15	1.2	1.25	V
$V_{HCP-UPPER}$	Hiccup counter upper threshold	RES rising		4.2		V
		RES rising, V_{VIN} = V_{VCC} = 4.5 V		3.6		V
$V_{HCP-LOWER}$	Hiccup counter lower threshold	RES falling		2.15		V
		RES falling, V_{VIN} = V_{VCC} = 4.5 V		1.85		V
$I_{RES-SOURCE1}$	RES current source1	Fault-state charging current	20	30	40	µA
$I_{RES-SINK1}$	RES current sink1	Normal-state discharging current		5		µA
$I_{RES-SOURCE2}$	RES current source2	Hiccup-mode off-time charging current		10		µA
$I_{RES-SINK2}$	RES current sink2	Hiccup-mode off-time discharging current		5		µA
	Hiccup cycle			8		Cycles
	RES discharge switch R_{DS-ON}			40		Ω
	Ratio of hiccup mode off-time to restart delay time			122		
HO GATE DRIVER						
V_{OHH}	HO high-state voltage drop	I_{HO} = –100 mA, V_{OHH} = V_{BST} –V_{HO}		0.15	0.24	V
V_{OLH}	HO low-state voltage drop	I_{HO} = 100 mA, V_{OLH} = V_{HO} –V_{SW}		0.1	0.18	V
	HO rise time (10% to 90%)	C_{LOAD} = 4700 pF, V_{BST} = 12 V		25		ns
	HO fall time (90% to 10%)	C_{LOAD} = 4700 pF, V_{BST} = 12 V		20		ns
I_{OHH}	Peak HO source current	V_{HO} = 0 V, V_{SW} = 0 V, V_{BST} = 4.5 V		0.8		A
		V_{HO} = 0 V, V_{SW} = 0 V, V_{BST} = 7.6 V		1.9		A
I_{OLH}	Peak HO sink current	V_{HO} = V_{BST} = 4.5 V		1.9		A
		V_{HO} = V_{BST}= 7.6 V		3.2		A
I_{BST}	BST charge pump sourcing current	V_{VIN} = V_{SW} = 9. V , V_{BST} - V_{SW} = 5 V	100	200		µA
	BST charge pump regulation	B_{ST} to SW, I_{BST}= –70 µA, V_{VIN} = V_{SW} = 9 V	5.3	6.2	6.75	V
		B_{ST} to SW, I_{BST} = –70 µA, V_{VIN} = V_{SW} = 12 V	7	8.5	9	V
	BST to SW undervoltage		2	3	3.5	V
	BST DC bias current	V_{BST} – V_{SW} = 12 V, V_{SW} = 0 V		30	45	µA

Electrical Characteristics (continued)

Unless otherwise specified, these specifications apply for –40°C ≤ T_J ≤ +125°C, V_{VIN} = 12 V, V_{VCC} = 8.3 V, R_T = 20 kΩ, no load on LO and HO. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LO GATE DRIVER						
V_{OHL}	LO high-state voltage drop	I_{LO} = –100 mA, V_{OHL} = V_{VCC} –V_{LO}		0.15	0.25	V
V_{OLL}	LO low-state voltage drop	I_{LO} = 100 mA, V_{OLL} = V_{LO}		0.1	0.17	V
	LO rise time (10% to 90%)	C_{LOAD} = 4700 pF		25		ns
	LO fall time (90% to 10%)	C_{LOAD} = 4700 pF		20		ns
I_{OHL}	Peak LO source current	V_{LO} = 0 V, V_{VCC} = 4.5 V		0.8		A
		V_{LO} = 0 V		2		A
I_{OLL}	Peak LO sink current	V_{LO} = V_{VCC} = 4.5 V		1.8		A
		V_{LO} = V_{VCC}		3.2		A
SWITCHING CHARACTERISTICS						
t_{DLH}	LO fall to HO rise delay	No load, 50% to 50%	50	80	115	ns
		No load, 50% to 50% (LM5122Z only)	50	80	145	
t_{DHL}	HO fall to LO rise delay	No load, 50% to 50%	60	80	105	ns
THERMAL						
T_{SD}	Thermal shutdown	Temperature rising		165		°C
	Thermal shutdown hysteresis			25		°C

6.6 Typical Characteristics

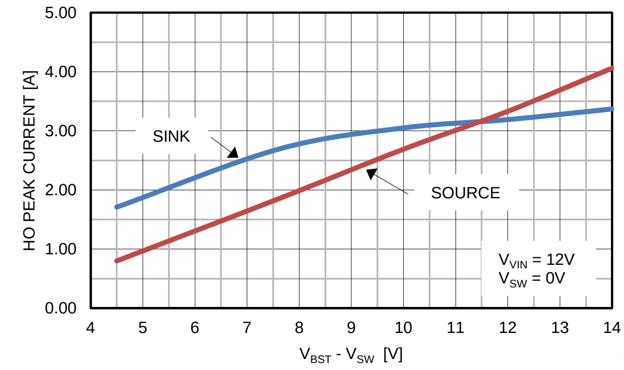


Figure 1. HO Peak Current vs V_{BST} - V_{SW}

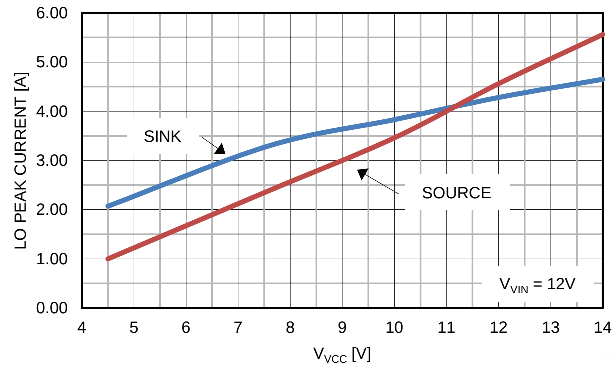


Figure 2. LO Peak Current vs V_{VCC}

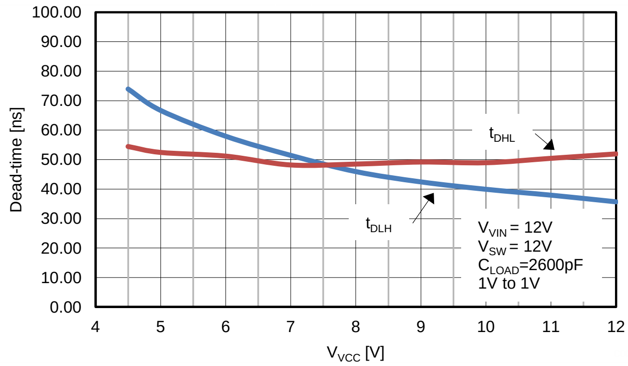


Figure 3. Dead Time vs V_{VCC}

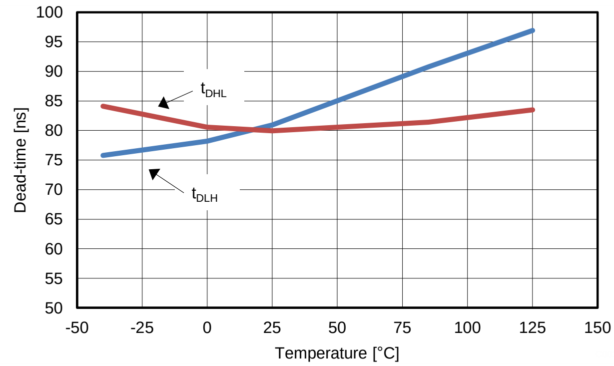


Figure 4. Dead Time vs Temperature

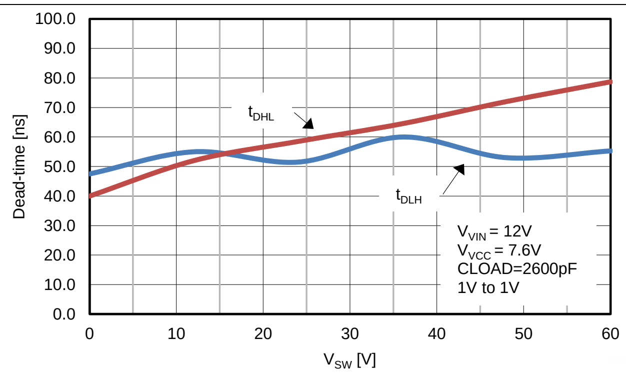


Figure 5. Dead Time vs V_{SW}

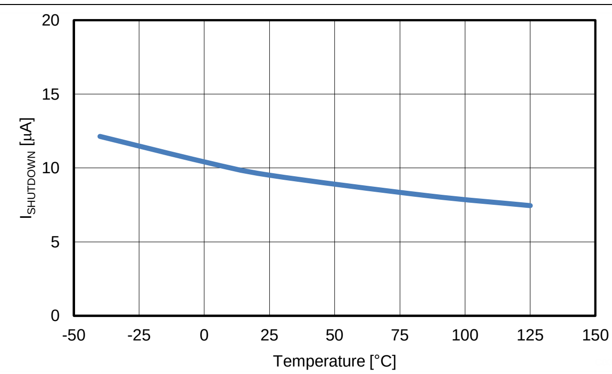


Figure 6. $I_{SHUTDOWN}$ vs Temperature

Typical Characteristics (continued)

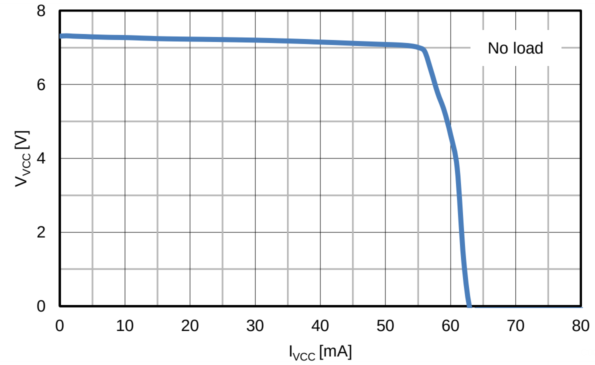


Figure 7. V_{VCC} vs I_{VCC}

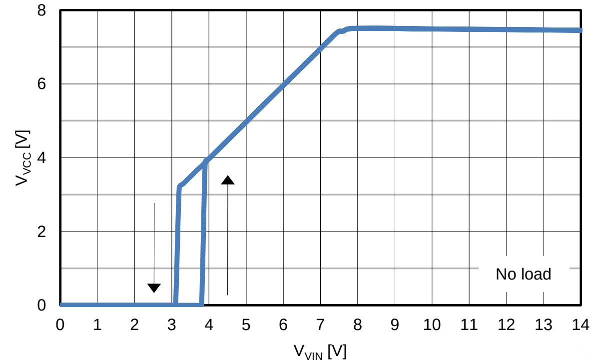


Figure 8. V_{VCC} vs V_{VIN}

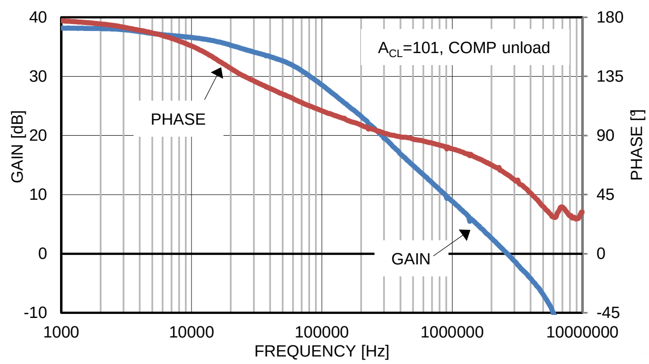


Figure 9. Error Amplifier Gain and Phase vs Frequency

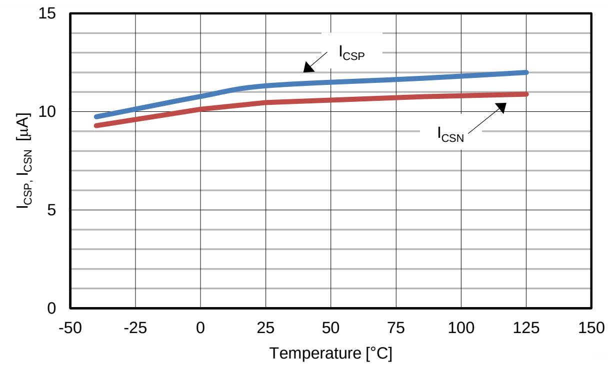


Figure 10. I_{CSP}, I_{CSN} vs Temperature

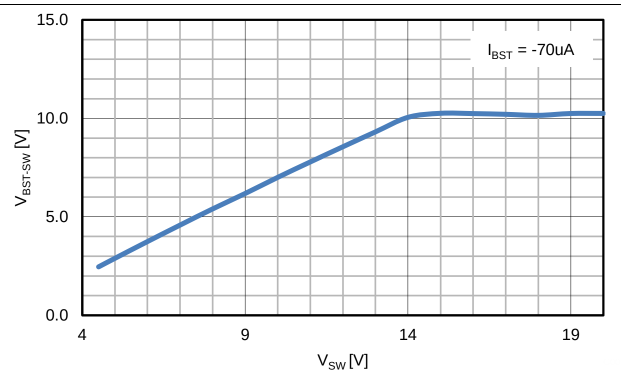


Figure 11. V_{BST-SW} vs V_{SW}

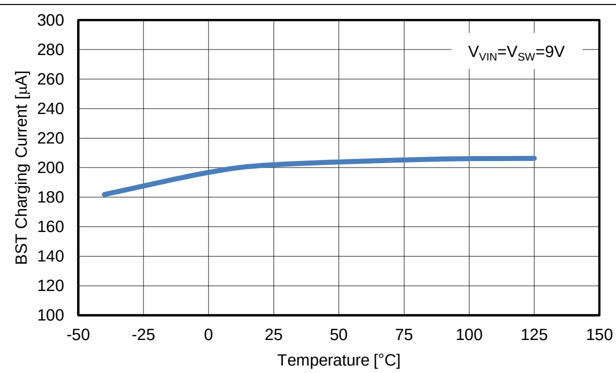


Figure 12. I_{BST} vs Temperature

Typical Characteristics (continued)

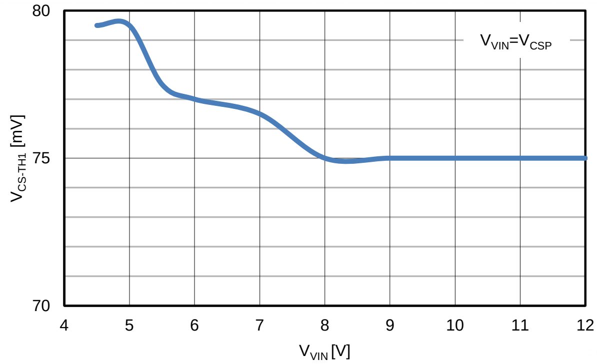


Figure 13. V_{CS-TH1} vs V_{VIN}

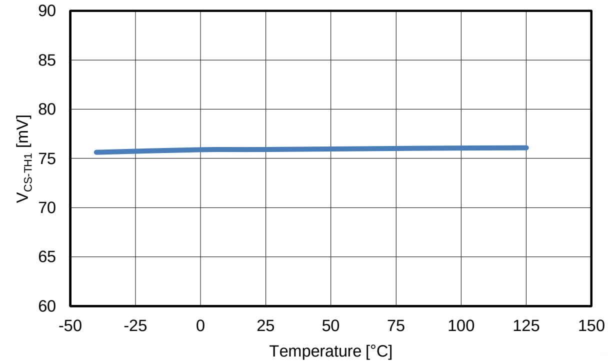


Figure 14. V_{CS-TH1} vs Temperature

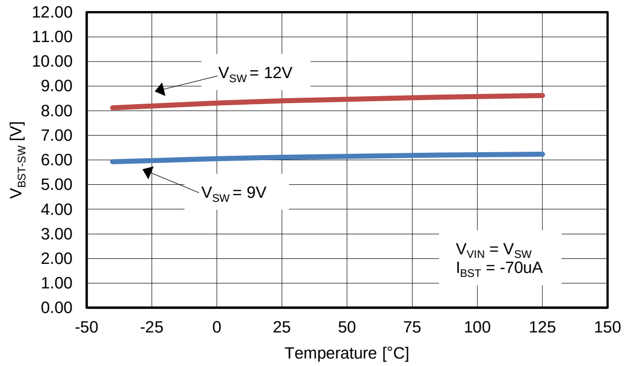


Figure 15. V_{BST-SW} vs Temperature

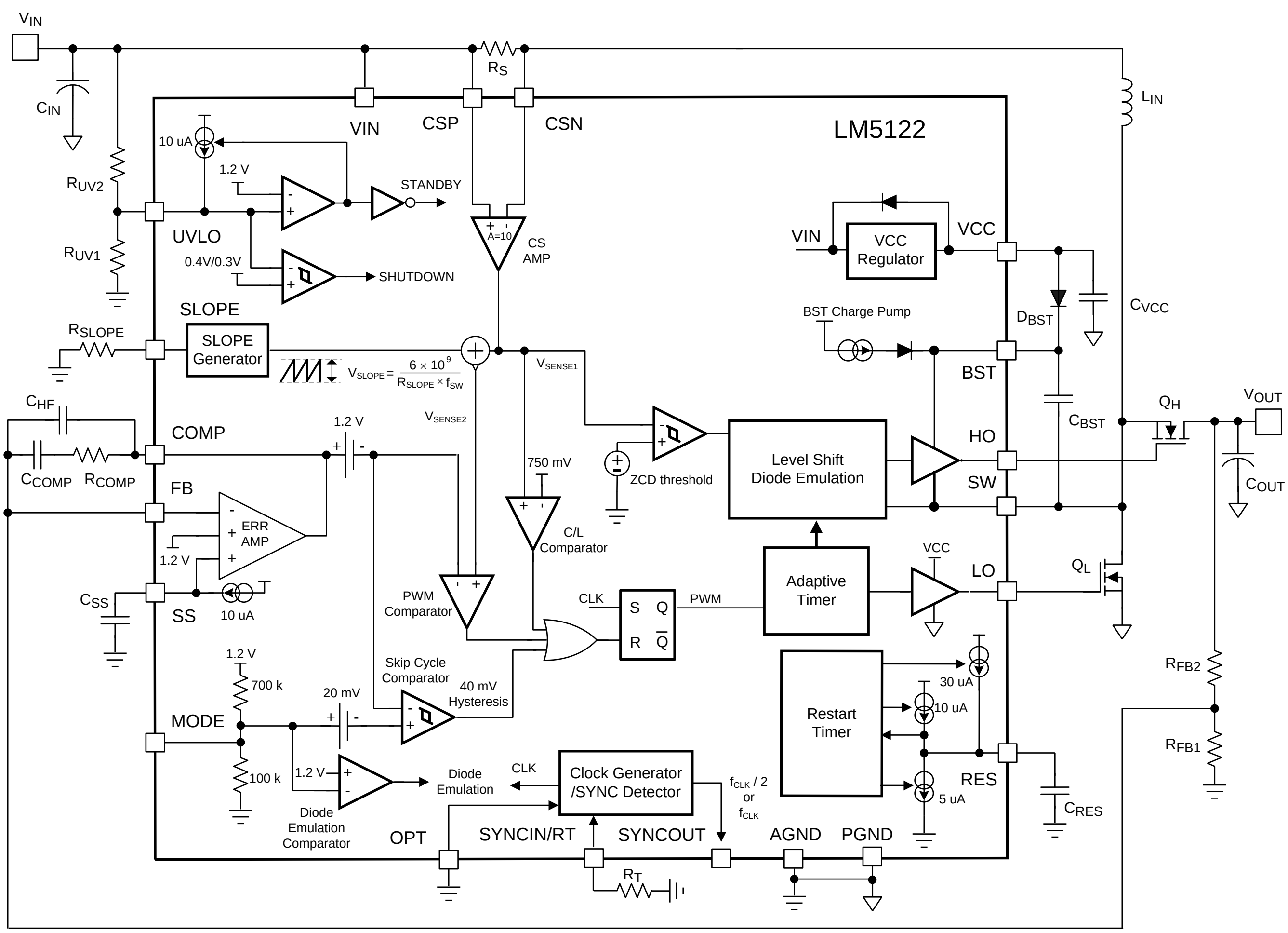
7 Detailed Description

7.1 Overview

The LM5122 wide input range synchronous boost controller features all of the functions necessary to implement a highly efficient synchronous boost regulator. The regulator control method is based upon peak current mode control. Peak current mode control provides inherent line feedforward and ease of loop compensation. This highly integrated controller provides strong high-side and low-side N-channel MOSFET drivers with adaptive dead-time control. The switching frequency is user programmable up to 1 MHz set by a single resistor or synchronized to an external clock. The 180º-shifted clock output of the LM5122 enables easy multi-phase configuration.

The control mode of high-side synchronous switch can be configured as either forced PWM (FPWM) or diode-emulation mode. Fault protection features include cycle-by-cycle current limiting, hiccup mode over load protection, thermal shutdown and remote shutdown capability by pulling down the UVLO pin. The UVLO input enables the controller when the input voltage reaches a user selected threshold, and provides a tiny 9-µA shutdown quiescent current when pulled low. The device is available in a 20 and 24-pin HTSSOP package featuring an exposed pad to aid in thermal dissipation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The LM5122 features a dual level UVLO circuit. When the UVLO pin voltage is less than the 0.4-V UVLO standby enable threshold, the LM5122 is in the shutdown mode with all functions disabled. The shutdown comparator provides 0.1 V of hysteresis to avoid chatter during transition. If the UVLO pin voltage is greater than 0.4 V and below 1.2 V during power up, the controller is in standby mode with the VCC regulator operational and no switching at the HO and LO outputs. This feature allows the UVLO pin to be used as a remote shutdown function by pulling the UVLO pin down below the UVLO standby enable threshold with an external open collector or open drain device.

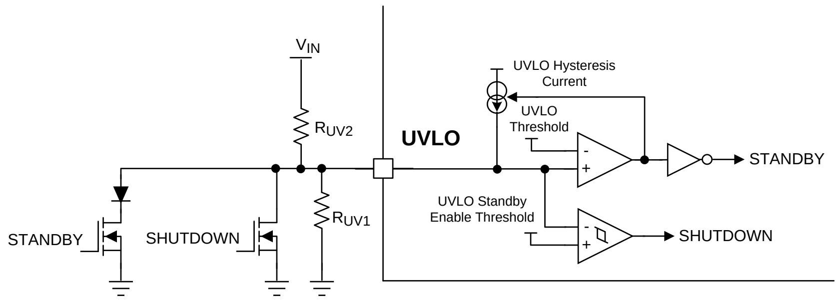


Figure 16. UVLO Remote Standby and Shutdown Control

If the UVLO pin voltage is above the 1.2-V UVLO threshold and VCC voltage exceeds the VCC UV threshold, a startup sequence begins. UVLO hysteresis is accomplished with an internal 10-µA current source that is switched on or off into the impedance of the UVLO setpoint divider. When the UVLO pin voltage exceeds 1.2 V, the current source is enabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.2-V UVLO threshold, the current source is disabled causing the voltage at the UVLO pin to quickly fall. In addition to the UVLO hysteresis current source, a 5-µs deglitch filter on both rising and falling edge of UVLO toggling helps preventing chatter upon power up or down.

An external UVLO setpoint voltage divider from the supply voltage to AGND is used to set the minimum input operating voltage of the regulator. The divider must be designed such that the voltage at the UVLO pin is greater than 1.2 V when the input voltage is in the desired operating range. The maximum voltage rating of the UVLO pin is 15 V. If necessary, the UVLO pin can be clamped with an external zener diode. The UVLO pin should not be left floating. The values of R_{UV1} and R_{UV2} can be determined from Equation 1 and Equation 2.

$$R_{UV2} = \frac{V_{HYS}}{10\mu A}[\Omega] \quad (1)$$

$$R_{UV1} = \frac{1.2V \times R_{UV2}}{V_{IN(STARTUP)} - 1.2V}[\Omega] \quad (2)$$

where

- V_{HYS} is the desired UVLO hysteresis
- $V_{IN(STARTUP)}$ is the desired startup voltage of the regulator during turn-on.

Typical shutdown voltage during turn-off can be calculated as follows:

$$V_{IN(SHUTDOWN)} = V_{IN(STARTUP)} - V_{HYS}[V] \quad (3)$$

7.3.2 High Voltage VCC Regulator

The LM5122 contains an internal high voltage regulator that provides typical 7.6 V VCC bias supply for the controller and N-channel MOSFET drivers. The input of VCC regulator, VIN, can be connected to an input voltage source as high as 65 V. The VCC regulator turns on when the UVLO pin voltage is greater than 0.4 V. When the input voltage is below the VCC setpoint level, the VCC output tracks VIN with a small dropout voltage. The output of the VCC regulator is current limited at 50 mA minimum.

Feature Description (continued)

Upon power-up, the VCC regulator sources current into the capacitor connected to the VCC pin. TI recommends a capacitance range for the VCC capacitor of 1 µF to 47 µF, and capacitance is recommended to be at least 10 times greater than C_{BST} value. When operating with a VIN voltage less than 6 V, the value of VCC capacitor must be 4.7 µF or greater.

The internal power dissipation of the LM5122 device can be reduced by supplying VCC from an external supply. If an external VCC bias supply exists and the voltage is greater than 9 V and below 14.5 V. The external VCC bias supply can be applied to the VCC pin directly through a diode, as shown in Figure 17.

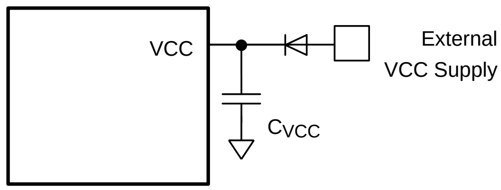


Figure 17. External Bias Supply when 9 V < V_{EXT}< 14.5 V

Shown in Figure 18 is a method to derive the VCC bias voltage with an additional winding on the boost inductor. This circuit must be designed to raise the VCC voltage above VCC regulation voltage to shut off the internal VCC regulator.

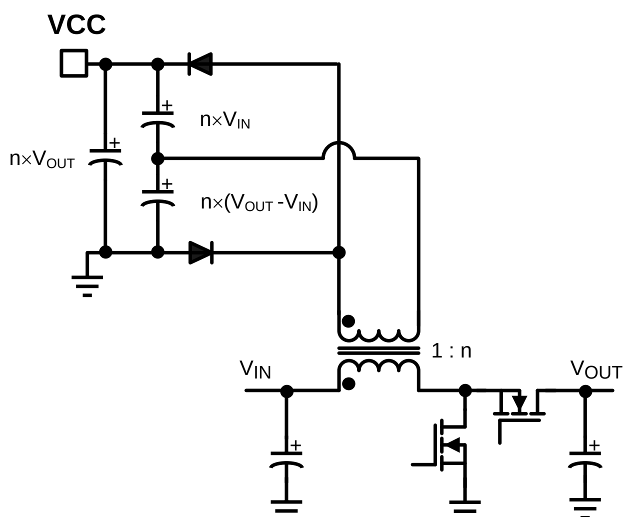


Figure 18. External Bias Supply using Transformer

The VCC regulator series pass transistor includes a diode between VCC and VIN that must not be fully forward biased in normal operation, as shown in Figure 19. If the voltage of the external VCC bias supply is greater than the VIN pin voltage, an external blocking diode is required from the input power supply to the VIN pin to prevent the external bias supply from passing current to the input supply through VCC. The need for the blocking diode should be evaluated for all applications when the VCC is supplied by the external bias supply. Especially, when the input power supply voltage is less than 4.5 V, the external VCC supply should be provided and the external blocking diode is required.

Feature Description (continued)

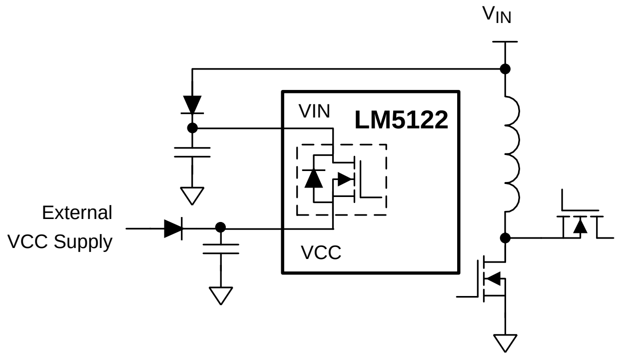


Figure 19. VIN Configuration when V_{VIN} < V_{VCC}

7.3.3 Oscillator

The LM5122 switching frequency is programmable by a single external resistor connected between the RT pin and the AGND pin. The resistor should be located very close to the device and connected directly to the RT pin and AGND pin. To set a desired switching frequency (f_{SW}), the resistor value can be calculated from Equation 4.

$$R_T = \frac{9 \times 10^9}{f_{SW}} [\Omega] \tag{4}$$

7.3.4 Slope Compensation

For duty cycles greater than 50%, peak current mode regulators are subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow duty cycles. This sub-harmonic oscillation can be eliminated by a technique, which adds an artificial ramp, known as slope compensation, to the sensed inductor current.

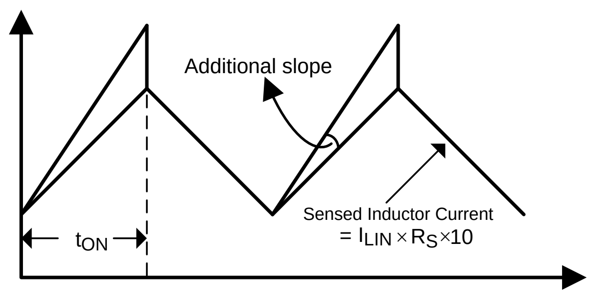


Figure 20. Slope Compensation

The amount of slope compensation is programmable by a single resistor connected between the SLOPE pin and the AGND pin. The amount of slope compensation can be calculated as follows:

$$V_{SLOPE} = \frac{6 \times 10^9}{f_{SW} \times R_{SLOPE}} \times D' [V]$$

where

- $$D' = 1 - \frac{V_{IN}}{V_{OUT}} \tag{5}$$

Feature Description (continued)

R_{SLOPE} value can be determined from Equation 6 at minimum input voltage:

$$R_{SLOPE} = \frac{L_{IN} \times 6 \times 10^9}{\left[K \times V_{OUT} - V_{IN(MIN)}\right] \times R_S \times 10}\left[\Omega\right]$$

where

- K=0.82~1 as a default (6)

From Equation 6, K can be calculated over the input range as follows:

$$K = \left(1 + \frac{L_{IN} \times 6 \times 10^9}{V_{IN} \times R_S \times 10 \times R_{SLOPE}}\right) \times D'$$

where

- $D' = \frac{V_{IN}}{V_{OUT}}$ (7)

In any case, K should be greater than at least 0.5. At higher switching frequency over 500 kHz, K factor is recommended to be greater than or equal to 1 because the minimum on-time affects the amount of slope compensation due to internal delays.

The sum of sensed inductor current and slope compensation should be less than COMP output high voltage (V_{OH}) for proper startup with load and proper current limit operation. This limits the minimum value of R_{SLOPE} to be:

$$R_{SLOPE} > \frac{5.7 \times 10^9}{f_{SW}} \times \left(1.2 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)\left[\Omega\right]$$

- This equation can be used in most cases

$$R_{SLOPE} > \frac{8 \times 10^9}{f_{SW}}\left[\Omega\right]$$

- Consider this conservative selection when $V_{IN(MIN)} < 5.5$ V

The SLOPE pin cannot be left floating.

7.3.5 Error Amplifier

The internal high-gain error amplifier generates an error signal proportional to the difference between the FB pin voltage and the internal precision 1.2-V reference. The output of the error amplifier is connected to the COMP pin allowing the user to provide a Type 2 loop compensation network.

R_{COMP}, C_{COMP} and C_{HF} configure the error amplifier gain and phase characteristics to achieve a stable voltage loop. This network creates a pole at DC, a mid-band zero (f_{Z_EA}) for phase boost, and a high frequency pole (f_{P_EA}). The minimum recommended value of R_{COMP} is 2 kΩ. See the *Feedback Compensation* section.

$$f_{Z\_EA} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}}\left[Hz\right] \quad (9)$$

$$f_{P\_EA} = \frac{1}{2\pi \times R_{COMP} \times \left(\frac{C_{COMP} \times C_{HF}}{C_{COMP} + C_{HF}}\right)}\left[Hz\right] \quad (10)$$

Feature Description (continued)

7.3.6 PWM Comparator

The PWM comparator compares the sum of sensed inductor current and slope compensation ramp to the voltage at the COMP pin through a 1.2-V internal COMP to PWM voltage drop, and terminates the present cycle when the sum of sensed inductor current and slope compensation ramp is greater than V_{COMP} –1.2 V.

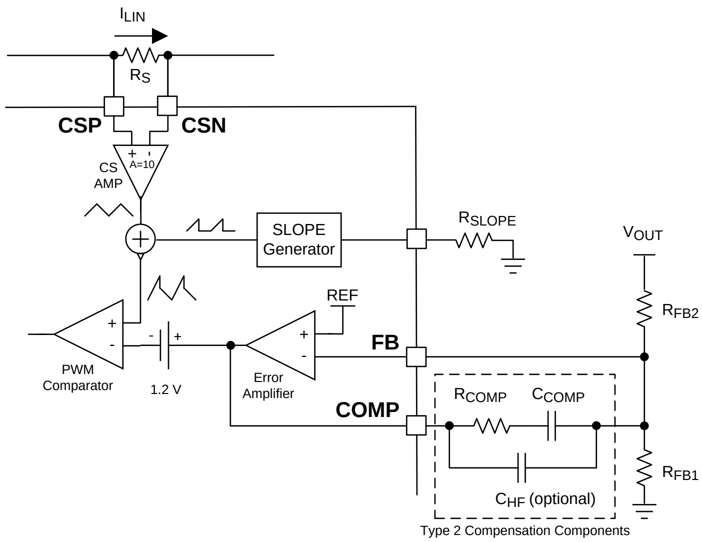


Figure 21. Feedback Configuration and PWM Comparator

7.3.7 Soft-Start

The soft-start feature helps the regulator to gradually reach the steady state operating point, thus reducing start-up stresses and surges. The LM5122 regulates the FB pin to the SS pin voltage or the internal 1.2-V reference, whichever is lower. The internal 10-µA soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin. This results in a gradual rise of the output voltage starting from the input voltage level to the target output voltage. Soft-start time (t_{SS}) which varies by the input supply voltage and is calculated from Equation 11.

$$t_{SS} = \frac{C_{SS} \times 1.2V}{10\mu A} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)[sec] \tag{11}$$

When the UVLO pin voltage is greater than the 1.2-V UVLO threshold and VCC voltage exceeds the VCC UV threshold, an internal 10-µA soft-start current source turns on. At the beginning of this soft-start sequence, allow V_{SS} to fall down below 25 mV using the internal SS pulldown switch. The SS pin can be pulled down by external switch to stop switching, but pulling up to enable switching is not allowed. The start-up delay (see Figure 22) must be long enough for high-side boot capacitor to be fully charged up by internal BST charge pump.

The value of C_{SS} must be large enough to charge the output capacitor during soft-start time.

$$C_{SS} > \frac{10\mu A \times V_{OUT}}{1.2V} \times \frac{C_{OUT}}{I_{OUT}}[F] \tag{12}$$

Feature Description (continued)

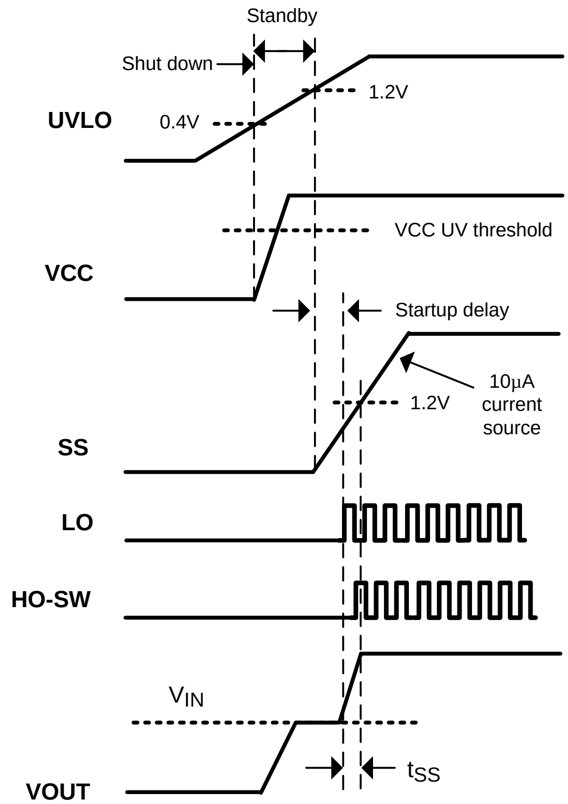


Figure 22. Startup Sequence

7.3.8 HO and LO Drivers

The LM5122 contains strong N-channel MOSFET gate drivers and an associated high-side level shifter to drive the external N-channel MOSFET switches. The high-side gate driver works in conjunction with an external boot diode D_{BST}, and bootstrap capacitor C_{BST}. During the on-time of the low-side N-channel MOSFET driver, the SW pin voltage is approximately 0 V and the C_{BST} is charged from VCC through the D_{BST}. TI recommends a 0.1-µF or larger ceramic capacitor, connected with short traces between the BST and SW pin.

The LO and HO outputs are controlled with an adaptive dead-time methodology which insures that both outputs are never enabled at the same time. When the controller commands LO to be enabled, the adaptive dead-time logic first disables HO and waits for HO-SW voltage to drop. LO is then enabled after a small delay (HO fall to LO rise delay). Similarly, the HO turnon is delayed until the LO voltage has discharged. HO is then enabled after a small delay (LO fall to HO rise delay). This technique insures adequate dead-time for any size N-channel MOSFET device, especially when VCC is supplied by a higher external voltage source. Be careful when adding series gate resistors, as this may decrease the effective dead-time.

Exercise care when selecting the N-channel MOSFET devices threshold voltage, especially if the VIN voltage range is below the VCC regulation level or a bypass operation is required. If the bypass operation is required, especially when output voltage is less than 12 V, a logic level device should be selected for the high-side N-channel MOSFET. During start-up at low input voltages, the low-side N-channel MOSFET switch's gate plateau voltage must be sufficient to completely enhance the N-channel MOSFET device. If the low-side N-channel MOSFET drive voltage is lower than the low-side N-channel MOSFET device gate plateau voltage during startup, the regulator may not start up properly and it may stick at the maximum duty cycle in a high power dissipation state. This condition can be avoided by selecting a lower threshold N-channel MOSFET switch or by increasing $V_{IN(STARTUP)}$ with the UVLO pin voltage programming.

Feature Description (continued)

7.3.9 Bypass Operation ($V_{OUT} = V_{IN}$)

The LM5122 allows 100% duty cycle operation for the high-side synchronous switch when the input supply voltage is equal to or greater than the target output voltage. An internal 200 μA BST charge pump maintains sufficient high-side driver supply voltage to keep the high-side N-channel MOSFET switch on without the power stage switching. The internal BST charge pump is enabled when the UVLO pin voltage is greater than 1.2 V and the VCC voltage exceeds the VCC UV threshold. The BST charge pump generates 5.3-V minimum BST to SW voltage when SW voltage is greater than 9 V. This requires minimum 9 V boost output voltage for proper bypass operation. The leakage current of the boot diode should be always less than the BST charge pump sourcing current to maintain a sufficient driver supply voltage at both low and high temperatures. Forced-PWM mode is the recommended PWM configuration when bypass operation is required.

7.3.10 Cycle-by-Cycle Current Limit

The LM5122 features a peak cycle-by-cycle current limit function. If the CSP to CSN voltage exceeds the 75-mV cycle-by-cycle current limit threshold, the current limit comparator immediately terminates the LO output.

For the case where the inductor current may overshoot, such as inductor saturation, the current limit comparator skips pulses until the current has decayed below the current limit threshold. Peak inductor current in current limit can be calculated as follows:

$$I_{PEAK(CL)} = \frac{75mV}{R_S}\left[A\right] \tag{13}$$

7.3.11 Clock Synchronization

The SYNCIN/RT pin can be used to synchronize the internal oscillator to an external clock. A positive going synchronization clock at the RT pin must exceed the RT sync rising threshold and negative going synchronization clock at RT pin must exceed the RT sync falling threshold to trip the internal synchronization pulse detector.

In Master1 mode, two types of configurations are allowed for clock synchronization. With the configuration in Figure 23, the frequency of the external synchronization pulse is recommended to be within +40% and –20% of the internal oscillator frequency programmed by the RT resistor. For example, 900-kHz external synchronization clock and 20-kΩ RT resistor are required for 450-kHz switching in master1 mode. The internal oscillator can be synchronized by AC coupling a positive edge into the RT pin. A 5-V amplitude pulse signal coupled through 100-pF capacitor is a good starting point. The RT resistor is always required with AC coupling capacitor with the Figure 23 configuration, whether the oscillator is free running or externally synchronized.

Care should be taken to ensure that the RT pin voltage does not go below –0.3 V at the falling edge of the external pulse. This may limit the duty cycle of external synchronization pulse. There is approximately 400-ns delay from the rising edge of the external pulse to the rising edge of LO.

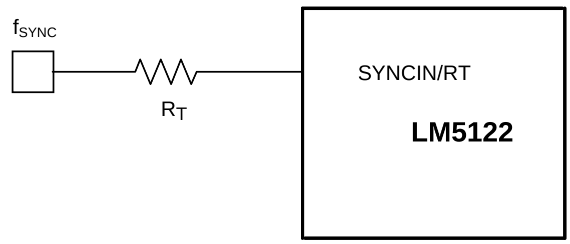


Figure 23. Oscillator Synchronization Through AC Coupling in Master1 Mode

With the configuration in Figure 24, the internal oscillator can be synchronized by connecting the external synchronization clock into the RT pin through RT resistor with free of the duty cycle limit. The output stage of the external clock source should be a low impedance totem-pole structure. Default logic state of f_{SYNC} must be low.

Feature Description (continued)

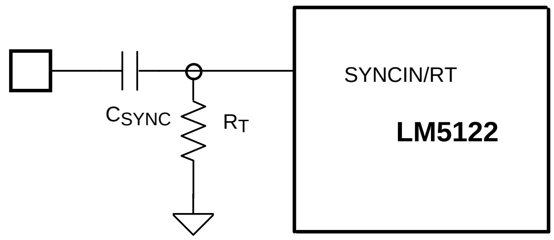


Figure 24. Oscillator Synchronization Through a Resistor in Master1 Mode

In master2 and slave modes, this external synchronization clock should be directly connected to the RT pin and always provided continuously. The internal oscillator frequency can be either of two times faster than switching frequency or the same as the switching frequency by configuring the combination of FB and OPT pins (see Table 1).

7.3.12 Maximum Duty Cycle

When operating with a high PWM duty cycle, the low-side N-channel MOSFET device is forced off each cycle. This forced LO off-time limits the maximum duty cycle of the controller. When designing a boost regulator with high switching frequency and high duty-cycle requirements, check the required maximum duty cycle. The minimum input supply voltage that can achieve the target output voltage is estimated from Equation 14 or Equation 15.

Use Equation 14 if V_{VCC} is greater than 5.5 V or V_{VIN} is greater than 6 V. For low voltage applications that do not satisfy either of these conditions use Equation 15.

$$V_{IN(MIN)} = f_{SW} \times V_{OUT} \times (400\,ns + margin)\ [V] \tag{14}$$

$$V_{IN(MIN)} = f_{SW} \times V_{OUT} \times (750\,ns + margin)\ [V] \tag{15}$$

In normal operation, about 100 ns of margin is recommended.

7.3.13 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the controller in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low-power shutdown mode, disabling the output drivers, disconnection switch and the VCC regulator. This feature is designed to prevent overheating and destroying the device.

7.4 Device Functional Modes

7.4.1 MODE Control (Forced-PWM Mode and Diode-Emulation Mode)

A fully synchronous boost regulator implemented with a high-side switch rather than a diode has the capability to sink current from the output in certain conditions such as light load, overvoltage or load transient. The LM5122 can be configured to operate in either forced-PWM mode (FPWM) or diode emulation mode.

In FPWM, reverse current flow in high-side N-channel MOSFET switch is allowed, and the inductor current conducts continuously at light or no load conditions. The benefit of the forced PWM mode is fast light load to heavy load transient response and constant frequency operation at light or no load conditions. To enable FPWM, connect the MODE pin to VCC or tie to a voltage greater than 1.2 V. In FPWM, reverse current flow is not limited.

In diode-emulation mode, current flow in the high-side switch is only permitted in one direction (source to drain). Turnon of the high-side switch is allowed if CSP to CSN voltage is greater than 7 mV rising threshold of zero current detection during low-side switch on-time. If CSP to CSN voltage is less than 6-mV falling threshold of zero current detection during high-side switch on-time, reverse current flow from output to input through the high-side N-channel MOSFET switch is prevented and discontinuous conduction mode of operation is enabled by latching off the high-side N-channel MOSFET switch for the remainder of the PWM cycle. A benefit of the diode emulation is lower power loss at light load conditions.

Device Functional Modes (continued)

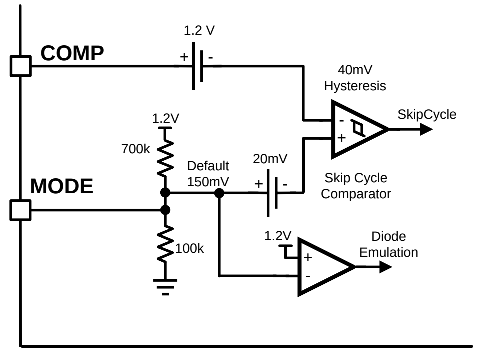


Figure 25. MODE Selection

During start-up the LM5122 forces diode emulation, for start-up into a pre-biased load, while the SS pin voltage is less than 1.2 V. Forced diode emulation is terminated by a pulse from PWM comparator when SS is greater than 1.2 V. If there are no LO pulses during the soft-start period, a 350-ns one-shot LO pulse is forced at the end of soft start to help charge the boot strap capacitor. Due to the internal current sense delay, configuring the LM5122 for diode emulation mode must be carefully evaluated if the inductor current ripple ratio is high and when operating at very high switching frequency. The transient performance during full load to no load in FPWM mode should also be verified.

7.4.2 MODE Control (Skip-Cycle Mode and Pulse-Skipping Mode)

Light load efficiency of the regulator typically drops as the losses associated with switching and bias currents of the converter become a significant percentage of the total power delivered to the load. In order to increase the light load efficiency the LM5122 provides two types of light load operation in diode-emulation mode.

The skip-cycle mode integrated into the LM5122 controller reduces switching losses and improves efficiency at light-load condition by reducing the average switching frequency. Skip-cycle operation is achieved by the skip cycle comparator. When a light-load condition occurs, the COMP pin voltage naturally decreases, reducing the peak current delivered by the regulator. During COMP voltage falling, the skip-cycle threshold is defined as V_{MODE} –20 mV and during COMP voltage rising, it is defined as V_{MODE} +20 mV. There is 40mV of internal hysteresis in the skip cycle comparator.

When the voltage at PWM comparator input falls below V_{MODE} –20 mV, both HO and LO outputs are disabled. The controller continues to skip switching cycles until the voltage at PWM comparator input increases to V_{MODE} + 20 mV, demanding more inductor current. The number of cycles skipped depends upon the load and the response time of the frequency compensation network. The internal hysteresis of skip-cycle comparator helps to produce a long skip cycle interval followed by a short burst of pulses. An internal 700-kΩ pullup and 100-kΩ pulldown resistor sets the MODE pin to 0.15 V as a default. Because the peak current limit threshold is set to 750 mV, the default skip threshold corresponds to approximately 17% of the peak level. In practice the skip level is lower due to the added slope compensation. By adding an external pullup resistor to SLOPE or VCC pin or adding an external pulldown resistor to the ground, the skip cycle threshold can be programmed. Because the skip cycle comparator monitors the PWM comparator input which is proportional to the COMP voltage, skip-cycle operation is not recommended when the bypass operation is required.

Conventional pulse-skipping operation can be achieved by connecting the MODE pin to ground. The negative 20-mV offset at the positive input of skip-cycle comparator ensures the skip-cycle comparator does not trigger in normal operation. At light or no load conditions, the LM5122 skips LO pulses if the pulse width required by the regulator is less than the minimum LO on-time of the device. Pulse skipping appears as a random behavior as the error amplifier struggles to find an average pulse width for LO in order to maintain regulation at light or no load conditions.

Device Functional Modes (continued)

7.4.3 Hiccup-Mode Overload Protection

If cycle-by-cycle current limit is reached during any cycle, a 30-µA current is sourced into the RES capacitor for the remainder of the clock cycle. If the RES capacitor voltage exceeds the 1.2-V restart threshold, a hiccup mode over load protection sequence is initiated; The SS capacitor is discharged to GND, both LO and HO outputs are disabled, the voltage on the RES capacitor is ramped up and down between 2-V hiccup counter lower threshold and 4-V hiccup counter upper threshold eight times by 10-µA charge and 5-µA discharge currents. After the eighth cycles, the SS capacitor is released and charged by the 10-µA soft-start current again. If a 3-V zener diode is connected in parallel with the RES capacitor, the regulator enters into the hiccup-mode off mode and then never restarts until UVLO shutdown is cycled. Connect RES pin directly to the AGND when the hiccup-mode operation is not used.

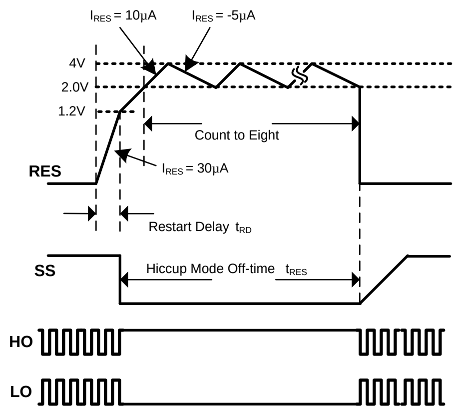


Figure 26. Hiccup Mode Overload Protection

7.4.4 Slave Mode and SYNCOUT

The LM5122 is designed to easily implement dual (or higher) phase boost converters by configuring one controller as a master and all others as slaves. Slave mode is activated by connecting the FB pin to the VCC pin. The FB pin is sampled during initial power-on and if a slave configuration is detected, the state is latched. In the slave mode, the error amplifier is disabled and has a high impedance output, 10-µA hiccup-mode off-time charging current and 5-µA hiccup-mode off-time discharging current are disabled, 5-µA normal-state RES discharging current and 10-µA soft-start charging current are disabled, 30 µA fault-state RES charging current is changed to 35 µA. 10-µA UVLO hysteresis current source works the same as master mode. Also, in slave mode, the internal oscillator is disabled, and an external synchronization clock is required.

The SYNCOUT function provides a 180° phase shifted clock output, enabling easy dual-phase interleaved configuration. By directly connecting master1 SYNCOUT to slave1 SYNCIN, the switching frequency of slave controller is synchronized to the master controller with 180º phase shift. In master mode, if OPT pin is tied to GND, an internal oscillator clock divided by two with 50% duty cycle is provided to achieve an 180º phase-shifted operation in two phase interleaved configuration. Switching frequency of master controller is half of the external clock frequency with this configuration. If the OPT pin voltage is higher than 2.7-V OPT threshold or the pin is tied to VCC, SYNCOUT is disabled and the switching frequency of master controller becomes the same as the external clock frequency. An external synchronization clock should be always provided and directly connected to SYNCIN for master2, slave1 and slave2 configurations. See *Interleaved Boost Configuration* for detailed information.

Table 1. LM5122 Multiphase Configuration

MULTIPHASE CONFIGURATION	FB	OPT	ERROR AMPLIFIER	SWITCHING FREQUENCY	SYNCOUT
Master1	Feedback	GND	Enable	f_{SYNC}/2, Free running with RT resistor	f_{SYNC}/2, f_{SW} –180º
Slave1	VCC	GND	Disable	$f_{SYNC,}$ No free running	Disable
Master2	Feedback	VCC	Enable	$f_{SYNC,}$ No free running	Disable
Slave2	VCC	VCC	Disable	f_{SYNC}/2, No free running	f_{SYNC}/2, f_{SW} –180º

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5122 device is a step-up dc-dc converter. The device is typically used to convert a lower dc voltage to a higher dc voltage. Use the following design procedure to select component values for the LM5122 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.1.1 Feedback Compensation

The open loop response of a boost regulator is defined as the product of modulator transfer function and feedback transfer function. When plotted on a dB scale, the open loop gain is shown as the sum of modulator gain and feedback gain. The modulator transfer function of a current mode boost regulator including a power stage transfer function with an embedded current loop can be simplified as one pole, one zero, and one right-half-plane (RHP) zero system.

Modulator transfer function is defined as follows:

$$\frac{\hat{V}_{OUT}(s)}{\hat{V}_{COMP}(s)} = A_M \times \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\times\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)}$$

where

- $A_M(\text{Modulator DC gain}) = \frac{R_{LOAD}}{R_{S\_EQ} \times A_S} \times \frac{D'}{2}$
- $\omega_{P\_LF}(\text{Load pole}) = \frac{2}{R_{LOAD} \times C_{OUT}}$
- $\omega_{Z\_ESR}(\text{ESR zero}) = \frac{1}{R_{ESR} \times C_{OUT}}$
- $\omega_{Z\_RHP}(\text{RHP zero}) = \frac{R_{LOAD} \times (D')^2}{L_{IN\_EQ}}$
- $L_{IN\_EQ} = \frac{L_{IN}}{n}, R_{S\_EQ} = \frac{R_S}{n}$
- n is the number of the phase. (16)

If the equivalent series resistance (ESR) of C_{OUT} (R_{ESR}) is small enough and the RHP zero frequency is far away from the target crossover frequency, the modulator transfer function can be further simplified to one pole system and the voltage loop can be closed with only two loop compensation components, R_{COMP} and C_{COMP}, leaving a single pole response at the crossover frequency. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

The feedback transfer function includes the feedback resistor divider and loop compensation of the error amplifier. R_{COMP}, C_{COMP}, and optional C_{HF} configure the error amplifier gain and phase characteristics, create a pole at origin, a low frequency zero and a high frequency pole.

Feedback transfer function is defined as follows:

Application Information (continued)

$$-\frac{\hat{V}_{COMP}}{\hat{V}_{OUT}} = A_{FB} \times \frac{1+\frac{s}{\omega_{Z\_EA}}}{s \times \left(1+\frac{s}{\omega_{P\_EA}}\right)}$$

where

- $A_{FB}(\text{Feedback DC gain}) = \frac{1}{R_{FB2} \times (C_{COMP} + C_{HF})}$
- $\omega_{Z\_EA}(\text{Low frequency zero}) = \frac{1}{R_{COMP} \times C_{COMP}}$
- $\omega_{P\_EA}(\text{High frequency pole}) = \frac{1}{R_{COMP} \times C_{HF}}$ (17)

The pole at the origin minimizes the output steady state error. Place the low frequency zero to cancel the load pole of the modulator. The high frequency pole can be used to cancel the zero created by the output capacitor ESR or to decrease noise susceptibility of the error amplifier. By placing the low frequency zero an order of magnitude less than the crossover frequency, the maximum amount of phase boost can be achieved at the crossover frequency. The high frequency pole should be placed beyond the crossover frequency since the addition of C_{HF} adds a pole in the feedback transfer function.

The crossover frequency (open loop bandwidth) is usually selected between one twentieth and one fifth of the f_{SW}. In a simplified formula, the estimated crossover frequency can be defined as:

$$f_{CROSS} = \frac{R_{COMP}}{\pi \times R_{S\_EQ} \times R_{FB2} \times A_S \times C_{OUT}} \times D' \text{ [Hz]}$$

where

- $D' = \frac{V_{IN}}{V_{OUT}}$ (18)

For higher crossover frequency, R_{COMP} can be increased, while proportionally decreasing C_{COMP}. Conversely, decreasing R_{COMP} while proportionally increasing C_{COMP}, results in lower bandwidth while keeping the same zero frequency in the feedback transfer function.

The modulator transfer function can be measured by a network analyzer and the feedback transfer function can be configured for the desired open loop transfer function. If the network analyzer is not available, step load transient tests can be performed to verify acceptable performance. The step load goal is minimum overshoot/undershoot with a damped response.

8.1.2 Sub-Harmonic Oscillation

Peak current mode regulator can exhibit unstable behavior when operating above 50% duty cycle. This behavior is known as sub-harmonic oscillation and is characterized by alternating wide and narrow pulses at the SW pin. Sub-harmonic oscillation can be prevented by adding an additional slope voltage ramp (slope compensation) on top of the sensed inductor current. By choosing K ≥ 0.82~1, the sub-harmonic oscillation is eliminated even with wide varying input voltage.

In time-domain analysis, the steady-state inductor current starting from an initial point returns to the same point. When the amplitude of an end cycle current error (dI_1) caused by an initial perturbation (dI_0) is less than the amplitude of dI_0 or $dI_1/dI_0 > -1$, the perturbation naturally disappears after a few cycles. When $dI_1/dI_0 < -1$, the initial perturbation no longer disappear, it results in sub-harmonic oscillation in steady-state.

Application Information (continued)

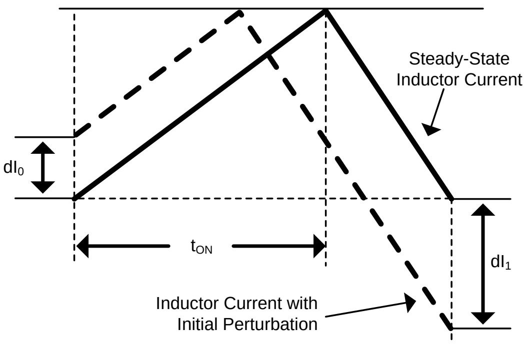


Figure 27. Effect of Initial Perturbation when $dI_1/dI_0 < -1$

dI_1/dI_0 can be calculated as:

$$\frac{dI_1}{dI_0} = 1 - \frac{1}{K} \tag{19}$$

The relationship between dI_1/dI_0 and K factor is illustrated graphically in Figure 28.

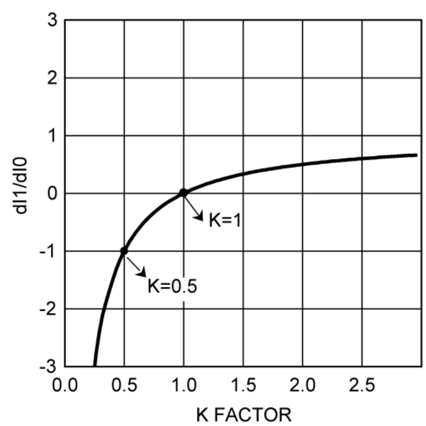


Figure 28. dI_1/dI_0 vs K Factor

The absolute minimum value of K is 0.5. When K < 0.5, the amplitude of dI_1 is greater than the amplitude of dI_0 and any initial perturbation results in sub-harmonic oscillation. If K = 1, any initial perturbation is removed in one switching cycle. This is known as one-cycle damping. When $–1 < dI_1/dI_0 < 0$, any initial perturbationis under-damped. Any perturbation is over-damped when $0 < dI_1/dI_0 < 1$.

In the frequency-domain, Q, the quality factor of sampling gain term in modulator transfer function, is used to predict the tendency for sub-harmonic oscillation, which is defined as:

$$Q = \frac{1}{\pi(K - 0.5)} \tag{20}$$

The relationship between Q and K factor is shown in Figure 29.

Application Information (continued)

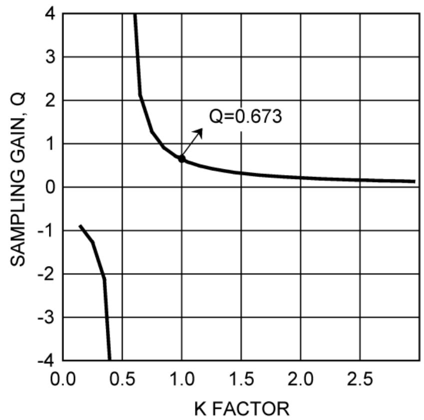


Figure 29. Sampling Gain Q vs K Factor

The recommended absolute minimum value of K is 0.5. High gain peaking when K is less than 0.5 results sub-harmonic oscillation at $f_{SW}/2$. A higher value of K factor may introduce additional phase shift near the crossover frequency, but has the benefit of reducing noise susceptibility in current loop. The maximum allowable value of K factor can be calculated by the maximum crossover frequency equation in frequency analysis formulas in Table 2.

Table 2. Boost Regulator Frequency Analysis

	SIMPLIFIED FORMULA	COMPREHENSIVE FORMULA (1)
MODULATOR TRANSER FUNCTION	$\frac{\hat{V}_{OUT}(s)}{\hat{V}_{COMP}(s)} = A_M \times \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\times\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)}$	$\frac{\hat{V}_{OUT}(s)}{\hat{V}_{COMP}(s)} = A_M \times \frac{\left(1+\frac{s}{\omega_{Z_{ESR}}}\right)\times\left(1-\frac{s}{\omega_{Z_{RHP}}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)\times\left(1+\frac{s}{\omega_{p\_ESR}}\right)\times\left(1+\frac{s}{\omega_{P\_HF}}+\frac{s^2}{\omega_n^{\ 2}}\right)}$
Modulator DC gain (2)	$A_M = \frac{R_{LOAD}}{R_{S\_EQ} \times A_S} \times \frac{D'}{2}$	
RHP zero (2)	$\omega_{Z\_RHP} = \frac{R_{LOAD} \times (D')^2}{L_{IN\_EQ}}$	
ESR zero	$\omega_{Z\_ESR} = \frac{1}{R_{ESR} \times C_{OUT}}$	$\omega_{Z\_ESR} = \frac{1}{R_{ESR1} \times C_{OUT1}}$
ESR pole	Not considered	$\omega_{P\_ESR} = \frac{1}{R_{ESR1} \times \left(C_{OUT1} // C_{OUT2}\right)}$
Dominant load pole	$\omega_{P\_LF} = \frac{2}{R_{LOAD} \times C_{OUT}}$	
Sampled gain inductor pole	Not considered	$\omega_{P\_HF} = \frac{f_{SW}}{K-0.5}$ or $\omega_{P\_HF} = Q \times \omega_n$
Quality factor	Not considered	$Q = \frac{1}{\pi(K-0.5)}$

(1) Comprehensive equation includes an inductor pole and a gain peaking at $f_{SW} / 2$, which is caused by sampling effect of the current mode control. Also, it assumes that a ceramic capacitor C_{OUT2} (No ESR) is connected in parallel with C_{OUT1}. R_{ESR1} represents ESR of C_{OUT1}.

(2) With multiphase configuration, $L_{IN\_EQ} = \frac{L_{IN}}{n}$, $R_{S\_EQ} = \frac{R_S}{n}$, $R_{LOAD} = \frac{V_{OUT}}{I_{OUT}\text{ of each phase} \times n}$, and C_{OUT} = C_{OUT} of each phase x n, where n = number of phases. As is the current sense amplifier gain.

Application Information (continued)

Table 2. Boost Regulator Frequency Analysis (continued)

	SIMPLIFIED FORMULA	COMPREHENSIVE FORMULA[1]
Sub-harmonic double pole	Not considered	$\omega_n = \frac{\omega_{SW}}{2} = \pi \times f_{SW}$ or $f_n = \frac{f_{SW}}{2}$
K factor	K = 1	$K = \left(1 + \frac{L_{IN} \times 6 \times 10^9}{V_{IN} \times R_S \times 10 \times R_{SLOPE}}\right) \times D'$
FEEDBACK TRANSFER FUNCTION	$-\frac{\hat{V}_{COMP}(s)}{\hat{V}_{OUT}(s)} = A_{FB} \times \frac{1 + \frac{s}{\omega_{Z\_EA}}}{s \times \left(1 + \frac{s}{\omega_{P\_EA}}\right)}$	
Feedback DC gain	$A_{FB} = \frac{1}{R_{FB2} \times (C_{COMP} + C_{HF})}$	
Mid-band Gain	$A_{FB\_MID} = \frac{R_{COMP}}{R_{FB2}}$	
Low frequency zero	$\omega_{Z\_EA} = \frac{1}{R_{COMP} \times C_{COMP}}$	
High frequency pole	$\omega_{P\_EA} = \frac{1}{R_{COMP} \times C_{HF}}$	$\omega_{P\_EA} = \frac{1}{R_{COMP} \times (C_{CHF} // C_{COMP})}$
OPEN LOOP RESPONSE	$T(s) = A_M \times A_{FB} \times \frac{\left(1 + \frac{s}{\omega_{Z\_ESR}}\right) \times \left(1 - \frac{s}{\omega_{Z\_RHP}}\right)}{\left(1 + \frac{s}{\omega_{P\_LF}}\right)} \times \frac{1 + \frac{s}{\omega_{Z\_EA}}}{s \times \left(1 + \frac{s}{\omega_{P\_EA}}\right)}$	$T(s) = A_M \times A_{FB} \times \frac{\left(1 + \frac{s}{\omega_{Z\_ESR}}\right) \times \left(1 - \frac{s}{\omega_{Z\_RHP}}\right)}{\left(1 + \frac{s}{\omega_{P\_LF}}\right) \times \left(1 + \frac{s}{\omega_{p\_ESR}}\right) \times \left(1 + \frac{s}{\omega_{P_{HF}}} + \frac{s^2}{\omega_n^2}\right)} \times \frac{1 + \frac{s}{\omega_{Z\_EA}}}{s \times \left(1 + \frac{s}{\omega_{P\_EA}}\right)}$
Crossover frequency [3] (Open loop band width)	$f_{CROSS} = \frac{R_{COMP}}{\pi \times R_{S\_EQ} \times R_{FB2} \times A_S \times C_{OUT}} \times D'$	Use graphic tool
Maximum cross over frequency[4]	$f_{CROSS\_MAX} = \frac{f_{SW}}{5}$ or $\frac{\omega_{Z\_RHP}}{2 \times \pi \times 4}$ whichever is smaller	$f_{CROSS\_MAX} = \frac{f_{SW}}{4 \times Q} \times \left(\sqrt{1 + 4 \times Q^2} - 1\right)$ or $\frac{\omega_{Z\_RHP}}{2 \times \pi \times 4}$, whichever is smaller

(3) Assuming $\omega_{Z\_EA} = \omega_{P\_LF}$, $\omega_{P\_EA} = \omega_{Z\_ESR}$, $f_{CROSS} < \frac{\omega_{Z\_RHP}}{2 \times \pi \times 10}$, $C_{COMP} = \frac{R_{LOAD} \times C_{OUT}}{4 \times R_{COMP}}$, and $D' = \frac{V_{IN}}{V_{OUT}}$.
(4) The frequency at which 45° phase shift occurs in modulator phase characteristics.

8.1.3 Interleaved Boost Configuration

Interleaved operation offers many advantages in single output, high current applications such as higher efficiency, lower component stresses and reduced input and output ripple. For dual phase interleaved operation, the output power path is split reducing the input current in each phase by one-half. Ripple currents in the input and output capacitors are reduced significantly since each channel operates 180 degrees out of phase from the other. Shown in Figure 30 is a normalized (I_{RMS}/I_{OUT}) output capacitor ripple current vs duty cycle for both a single phase and dual phase boost converter, where I_{RMS} is the output current ripple RMS.

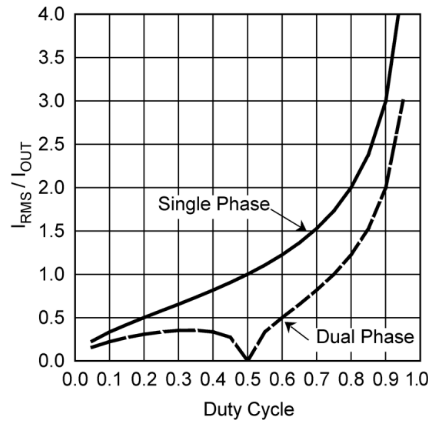


Figure 30. Normalized Output Capacitor RMS Ripple Current

To configure for dual phase interleaved operation, configure one device as a master and configure the other device in slave mode by connecting FB to VCC. Also connect COMP, UVLO, RES, SS and SYNCOUT on the master side to COMP, UVLO, RES, SS and SYNCIN on slave side, respectively. The compensation network is connected between master FB and the common COMP connection. The output capacitors of the two power stages are connected together at the common output.

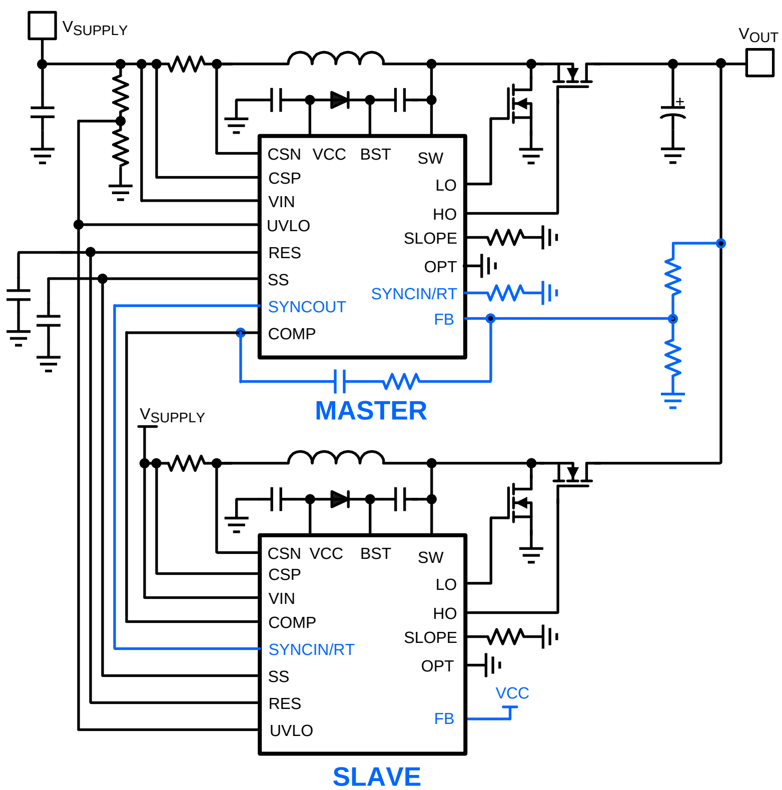


Figure 31. Dual Phase Interleaved Boost Configuration

Shown in Figure 32 is a dual phase timing diagram. The 180° phase shift is realized by connecting SYNCOUT on the master side to the SYNCIN on the slave side.

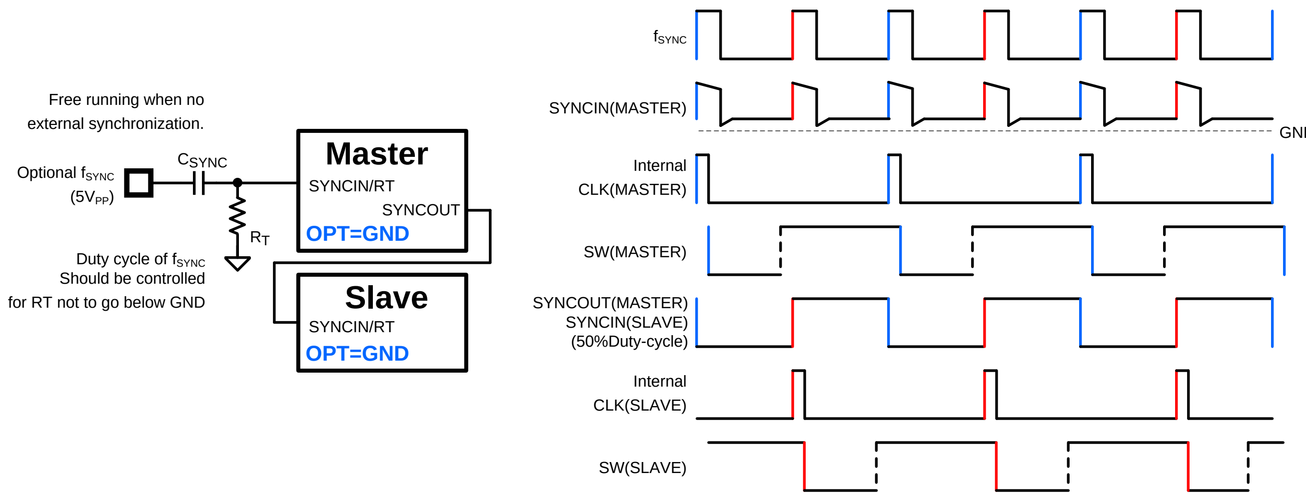


Figure 32. Dual Phase Configuration and Timing Diagram

Each channel is synchronized by an individual external clock in Figure 33. The SYNCOUT pin is used in Figure 34 requiring only one external clock source. A 50% duty cycle of external synchronization pulse should be always provided with this daisy chain configuration.

Current sharing between phases is achieved by sharing one error amplifier output of the master controller with the 3 slave controllers. Resistor sensing is a preferred method of current sensing to accurately balance the phase currents.

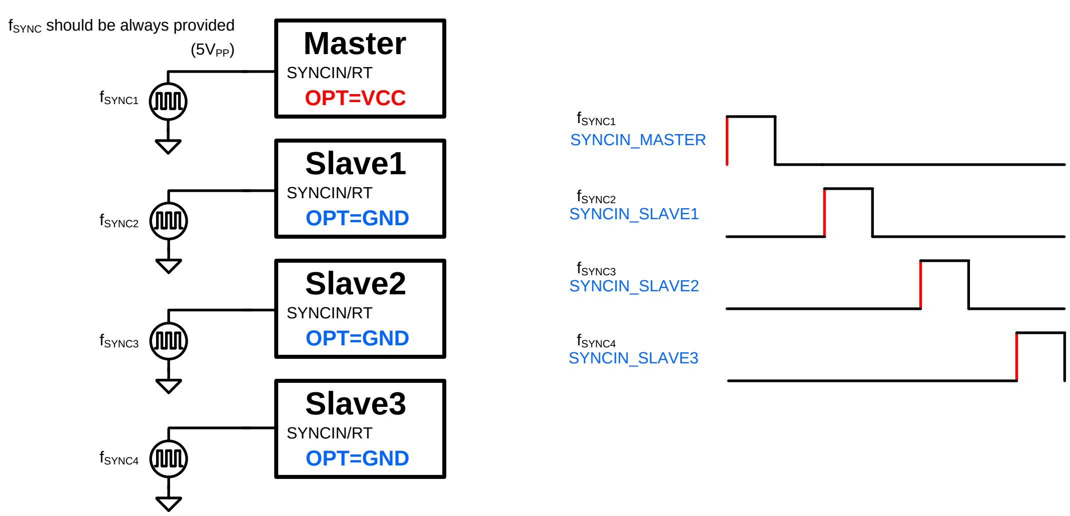


Figure 33. 4-Phase Timing Diagram Individual Clock

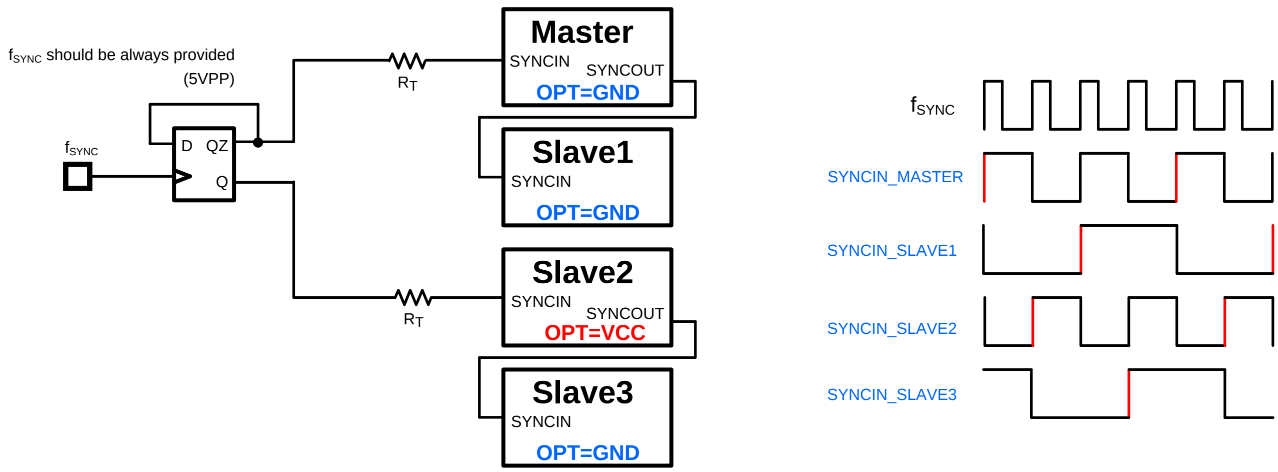


Figure 34. 4-Phase Timing Diagram Daisy Chain

8.1.4 DCR Sensing

For the applications requiring lowest cost with minimum conduction loss, inductor DC resistance (DCR) is used to sense the inductor current rather than using a sense resistor. Shown in Figure 35 is a DCR sensing configuration using two DCR sensing resistors and one capacitor.

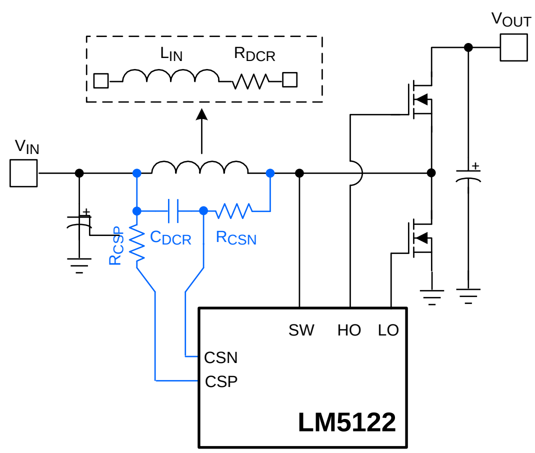


Figure 35. DCR Sensing

R_{CSN} and C_{DCR} selection must meet Equation 21 because this indirect current sensing method requires a time constant matching. C_{DCR} is usually selected to be in the range of 0.1 µF to 2.2 µF.

$$\frac{L_{IN}}{R_{DCR}} = C_{DCR} \times R_{CSN} \tag{21}$$

Smaller value of R_{CSN} minimizes the voltage drop caused by CSN bias current, but increases the dynamic power dissipation of R_{CSN}. The DC voltage drop of R_{CSN} can be compensated by selecting the same value of R_{CSP}, but the gain of current amplifier, which is typically 10, is affected by adding R_{CSP}. The gain of current amplifier with the DCR sensing network can be determined as:

$$A_{CS\_DCR} = 12.5\ \text{k}\Omega\, /\, (1.25\ \text{k}\Omega + R_{CSP}) \tag{22}$$

Due to the reduced accuracy of DCR sensing, TI recommends FPWM operation when DCR sensing is used.

8.1.5 Output Overvoltage Protection

Output overvoltage protection can be achieved by adding a simple external circuit. The output overvoltage protection circuit shown in Figure 36 shuts down the LM5122 when the output voltage exceeds the overvoltage threshold set by the zener diode.

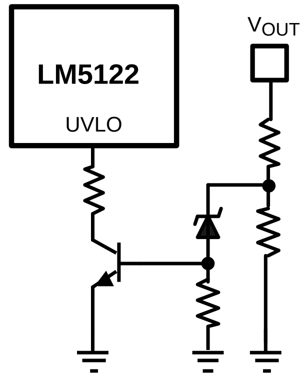


Figure 36. Output Overvoltage Protection

8.1.6 SEPIC Converter Simplified Schematic

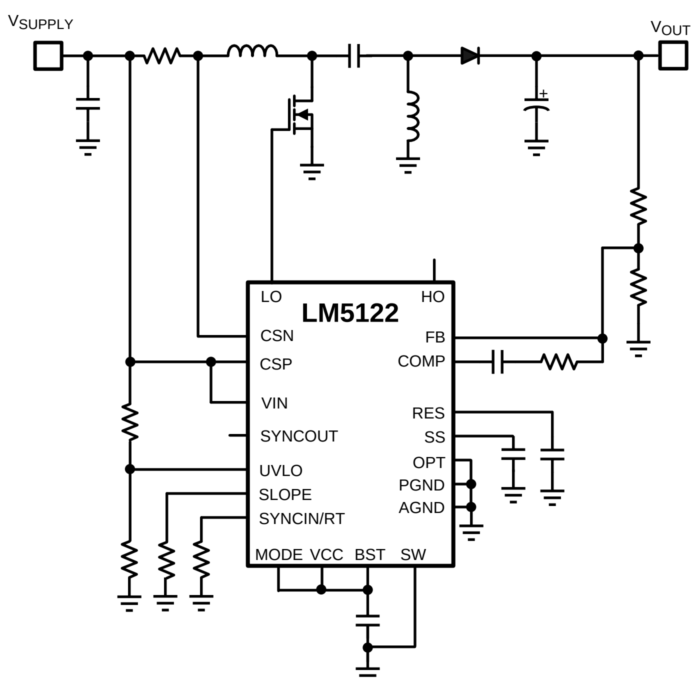


Figure 37. Sepic Converter Simplified Schematic

8.1.7 Non-Isolated Synchronous Flyback Converter Simplified Schematic

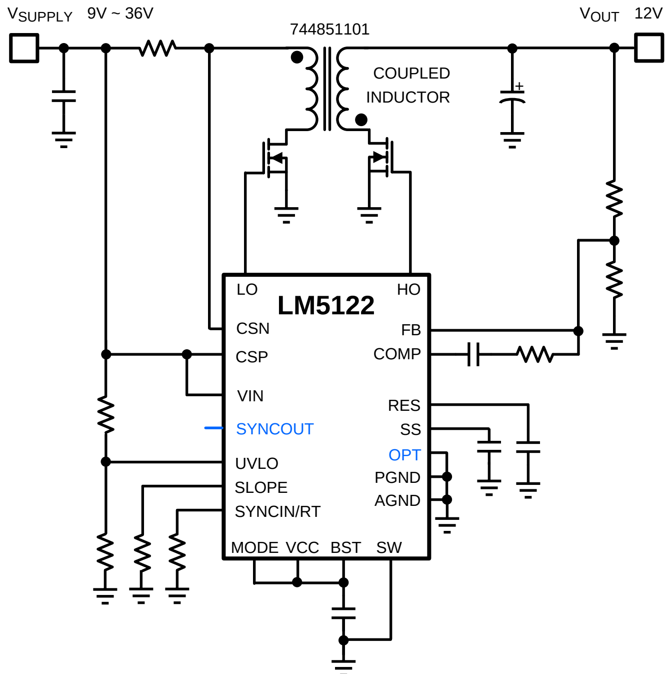


Figure 38. Non-Isolated Synchronous Flyback Converter Simplified Schematic

8.1.8 Negative to Positive Conversion

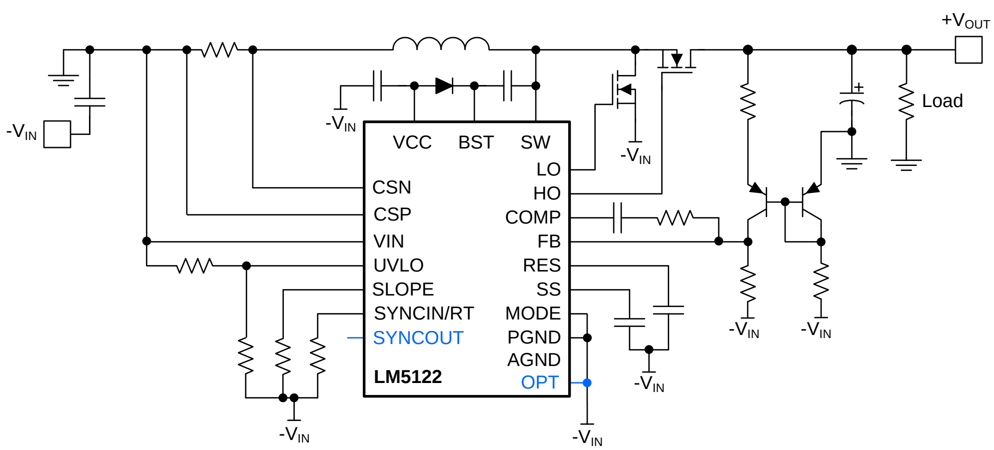


Figure 39. Negative to Positive Converter Simplified Schematic

8.2 Typical Application

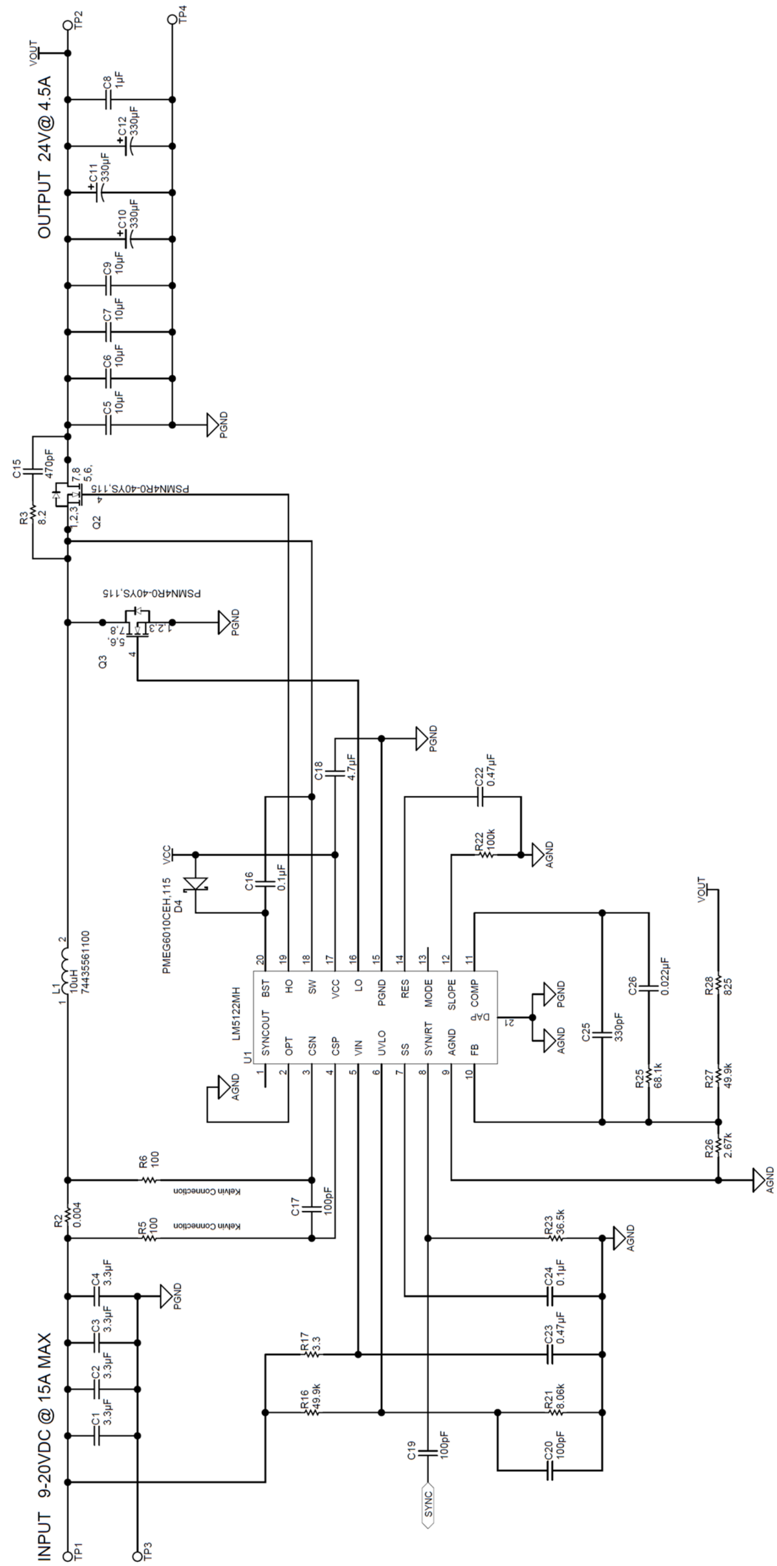


Figure 40. Single Phase Example Schematic

Typical Application (continued)

8.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
Output voltage (V_{OUT})	24 V
Full load current (I_{OUT})	4.5 A
Output Power	108 W
Minimum input voltage ($V_{IN(MIN)}$)	9 V
Typical input voltage ($V_{IN(TYP)}$)	12 V
Maximum input voltage ($V_{IN(MAX)}$)	20 V
Switching frequency (f_{SW})	250 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5122 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Timing Resistor R_T

Generally, higher frequency applications are smaller but have higher losses. Operation at 250 kHz is selected for this example as a reasonable compromise between small size and high-efficiency. The value of R_T for 250 kHz switching frequency is calculated as follows:

$$R_T = \frac{9 \times 10^9}{f_{SW}} = \frac{9 \times 10^9}{250\ \text{kHz}} = 36.0\ \text{k}\Omega \tag{23}$$

A standard value of 36.5 kΩ is chosen for R_T.

8.2.2.3 UVLO Divider R_{UV2}, R_{UV1}

The desired startup voltage and the hysteresis are set by the voltage divider R_{UV2}, R_{UV1}. The UVLO shutdown voltage should be high enough to enhance the low-side N-channel MOSFET switch fully. For this design, the startup voltage is set to 8.7 V which is 0.3 V below $V_{IN(MIN)}$. V_{HYS} is set to 0.5 V. This results 8.2 V of $V_{IN(SHUTDOWN)}$. The values of R_{UV2}, R_{UV1} are calculated as follows:

$$R_{UV2} = \frac{V_{HYS}}{I_{HYS}} = \frac{0.5\ \text{V}}{10\ \mu\text{A}} = 50\ \text{k}\Omega \tag{24}$$

$$R_{UV1} = \frac{1.2\text{V} \times R_{UV2}}{V_{IN(STARTUP)} - 1.2\text{V}} = \frac{1.2\text{V} \times 50\ \text{k}\Omega}{8.7\text{V} - 1.2\text{V}} = 8\ \text{k}\Omega \tag{25}$$

A standard value of 49.9 kΩ is selected for R_{UV2}. R_{UV1} is selected to be a standard value of 8.06 kΩ.

8.2.2.4 Input Inductor L_{IN}

The inductor ripple current is typically set between 20% and 40% of the full load current, known as a good compromise between core loss and copper loss of the inductor. Higher ripple current allows for a smaller inductor size, but places more of a burden on the output capacitor to smooth the ripple voltage on the output. For this example, a ripple ratio (RR) of 0.25, 25% of the input current was chosen. Knowing the switching frequency and the typical output voltage, the inductor value can be calculated as follows:

$$L_{IN} = \frac{V_{IN}}{I_{IN} \times RR} \times \frac{1}{f_{SW}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) = \frac{12V}{\frac{108W}{12V} \times 0.25} \times \frac{1}{250\text{ kHz}} \times \left(1 - \frac{12V}{24V}\right) = 10.7\ \mu H \quad (26)$$

The closest standard value of 10 μH was chosen for L_{IN}.

The saturation current rating of inductor should be greater than the peak inductor current, which is calculated at the minimum input voltage and full load. 8.7 V startup voltage is used conservatively.

$$I_{PEAK} = I_{IN} + \frac{1}{2} \times \frac{V_{IN}}{L_{IN} \times f_{SW}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) = \frac{24V \times 4.5A}{8.7V} + \frac{1}{2} \times \frac{8.7V}{10\ \mu H \times 250\text{ kHz}} \times \left(1 - \frac{8.7V}{24V}\right) = 13.5\text{ A} \quad (27)$$

8.2.2.5 Current Sense Resistor R_S

The maximum peak input current capability should be 20~50% higher than the required peak current at low input voltage and full load, accounting for tolerances. For this example, 40% is margin is chosen.

$$R_S = \frac{V_{CS-TH1}}{I_{PEAK(CL)}} = \frac{75\text{ mV}}{13.5\text{ A} \times 1.4} = 3.97\text{ m}\Omega \quad (28)$$

A closest standard value of 4 mΩ is selected for R_S. The maximum power loss of R_S is calculated as follows.

$$P_{LOSS(RS)} = I^2R = (13.5\text{ A} \times 1.4)^2 \times 4\text{ m}\Omega = 1.43\text{ W} \quad (29)$$

8.2.2.6 Current Sense Filter R_{CSFP}, R_{CSFN}, C_{CS}

The current sense filter is optional. 100 pF of C_{CS} and 100 Ω of R_{CSFP}, R_{CSFN} are normal recommendations. Because CSP and CSN pins are high impedance, C_{CS} should be placed physically as close to the device.

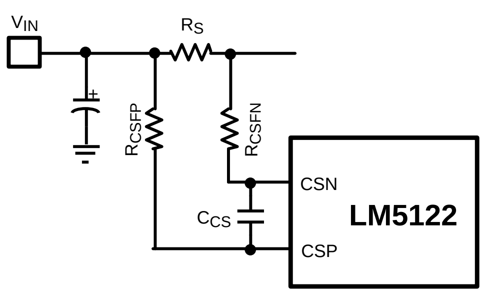


Figure 41. Current Sense Filter

8.2.2.7 Slope Compensation Resistor R_{SLOPE}

The K value is selected to be 1 at the minimum input voltage. R_{SLOPE} should be carefully selected so that the sum of sensed inductor current and slope compensation is less than COMP output high voltage.

$$R_{SLOPE} > \frac{8 \times 10^9}{f_{SW}} = \frac{8 \times 10^9}{250\text{ kHz}} = 32\text{ k}\Omega \quad (30)$$

$$R_{SLOPE} = \frac{L_{IN} \times 6 \times 10^9}{\left[K \times V_{OUT} - V_{IN(MIN)}\right] \times R_S \times 10} = \frac{10\ \mu H \times 6 \times 10^9}{(1 \times 24V - 9V) \times 4m\Omega \times 10} = 100\text{ k}\Omega \quad (31)$$

A closest standard value of 100 kΩ is selected for R_{SLOPE}.

8.2.2.8 Output Capacitor C_{OUT}

The output capacitors smooth the output voltage ripple and provide a source of charge during transient loading conditions. Also the output capacitors reduce the output voltage overshoot when the load is disconnected suddenly.

Ripple current rating of output capacitor should be carefully selected. In boost regulator, the output is supplied by discontinuous current and the ripple current requirement is usually high. In practice, the ripple current requirement can be dramatically reduced by placing high-quality ceramic capacitors earlier than the bulk aluminum capacitors close to the power switches.

The output voltage ripple is dominated by ESR of the output capacitors. Paralleling output capacitor is a good choice to minimize effective ESR and split the output ripple current into capacitors.

In this example, three 330 µF aluminum capacitors are used to share the output ripple current and source the required charge. The maximum output ripple current can be simply calculated at the minimum input voltage as follows:

$$I_{RIPPLE\_MAX(COUT)} = \frac{I_{OUT}}{2 \times \frac{V_{IN(MIN)}}{V_{OUT}}} = \frac{4.5A}{2 \times \frac{9V}{24V}} = 6A \tag{32}$$

Assuming 60 mΩ of ESR per an output capacitor, the output voltage ripple at the minimum input voltage is calculated as follows:

$$V_{RIPPLE\_MAX(COUT)} = \frac{I_{OUT}}{\frac{V_{IN(MIN)}}{V_{OUT}}} \times \left(R_{ESR} + \frac{1}{4 \times C_{OUT} \times f_{SW}}\right) = \frac{4.5A}{\frac{9V}{24V}} \times \left(\frac{60m\Omega}{3} + \frac{1}{4 \times 3 \times 330\ \mu F \times 250\ kHz}\right) = 0.252V \tag{33}$$

In practice, four 10-µF ceramic capacitors are additionally placed earlier than the bulk aluminum capacitors to reduce the output voltage ripple and split the output ripple current.

Due to the inherent path from input to output, unlimited inrush current can flow when the input voltage rises quickly and charges the output capacitor. The slew rate of input voltage rising should be controlled by a hot-swap or by starting the input power supply softly for the inrush current not to damage the inductor, sense resistor or high-side N-channel MOSFET switch.

8.2.2.9 Input Capacitor C_{IN}

The input capacitors smooth the input voltage ripple. Assuming high-quality ceramic capacitors are used for the input capacitors, the maximum input voltage ripple which happens when the input voltage is half of the output voltage can be calculated as follows:

$$V_{RIPPLE\_MAX(CIN)} = \frac{V_{OUT}}{32 \times L_{IN} \times C_{IN} \times f_{SW^2}} = \frac{24V}{32 \times 10\ \mu H \times 4 \times 3.3\ \mu F \times 250\ kHz^2} = 0.09V \tag{34}$$

The value of input capacitor is also a function of source impedance, the impedance of source power supply. The more input capacitor will be required to prevent a chatter condition upon power up if the impedance of source power supply is not enough low.

8.2.2.10 VIN Filter R_{VIN}, C_{VIN}

An R-C filter (R_{VIN}, C_{VIN}) on VIN pin is optional. It is not required if C_{IN} capacitors are high-quality ceramic capacitors and placed physically close to the device. The filter helps to prevent faults caused by high frequency switching noise injection into the VIN pin. A 0.47 µF ceramic capacitor is used this example. 3 Ω of R_{VIN} and 0.47 µF of C_{VIN} are normal recommendations. A larger filter with 2.2 µ~4.7 µF C_{VIN} is recommended when the input voltage is lower than 8 V or the required duty cycle is close to the maximum duty cycle limit.

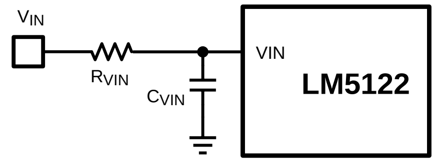


Figure 42. VIN Filter

8.2.2.11 Bootstrap Capacitor C_{BST} and Boost Diode D_{BST}

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side N-channel MOSFET device gate during each cycle's turn-on and also supplies recovery charge for the bootstrap diode. These current peaks can be several amperes. The recommended value of the bootstrap capacitor is 0.1 µF. C_{BST} must be a good-quality, low-ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. The minimum value for the bootstrap capacitor is calculated as follows:

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}} [F]$$

where

- Q_G is the high-side N-channel MOSFET gate charge
- ΔV_{BST} is the tolerable voltage droop on C_{BST}, which is typically less than 5% of VCC or 0.15 V, conservatively (35)

In this example, the value of the BST capacitor (C_{BST}) is 0.1 µF.

The voltage rating of D_{BST} must be greater than the peak SW node voltage plus 16 V. A low leakage diode is mandatory for the bypass operation. The leakage current of D_{BST} must be low enough for the BST charge pump to maintain a sufficient high-side driver supply voltage at high temperature. A low leakage diode also prevents the possibility of excessive VCC voltage during shutdown, in high output voltage applications. If the leakage is excessive, a zener VCC clamp or bleed resistor may be required. High-side driver supply voltage must be greater than the high-side N-channel MOSFET switch's gate plateau at the minimum input voltage.

8.2.2.12 VCC Capacitor C_{VCC}

The primary purpose of the VCC capacitor is to supply the peak transient currents of the LO driver and bootstrap diode as well as provide stability for the VCC regulator. These peak currents can be several amperes. The value of C_{VCC} must be at least 10 times greater than the value of C_{BST} and should be a good-quality, low-ESR, ceramic capacitor. Place C_{VCC} close to the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 4.7 µF was selected for this design example.

8.2.2.13 Output Voltage Divider R_{FB1}, R_{FB2}

R_{FB1} and R_{FB2} set the output voltage level. The ratio of these resistors is calculated as follows:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{1.2V} - 1 \quad (36)$$

The ratio between R_{COMP} and R_{FB2} determines the mid-band gain, A_{FB_MID}. A larger value for R_{FB2} may require a corresponding larger value for R_{COMP}. R_{FB2} should be large enough to keep the total divider power dissipation small. 49.9 kΩ in series with 825 Ω was chosen for high-side feedback resistors in this example, which results in a R_{FB1} value of 2.67 kΩ for 24-V output.

8.2.2.14 Soft-Start Capacitor C_{SS}

The soft-start time (t_{SS}) is the time for the output voltage to reach the target voltage from the input voltage. The soft-start time is not only proportional with the soft-start capacitor, but also depends on the input voltage. With 0.1 µF of C_{SS}, the soft-start time is calculated as follows:

$$t_{SS(MIN)} = \frac{C_{SS} \times 1.2V}{I_{SS}} \times \left(1 - \frac{V_{IN(MAX)}}{V_{OUT}}\right) = \frac{0.1\,\mu F \times 1.2V}{10\,\mu A} \times \left(1 - \frac{20V}{24V}\right) = 2 \text{ msec} \quad (37)$$

$$t_{SS(MAX)} = \frac{C_{SS} \times 1.2V}{I_{SS}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right) = \frac{0.1\,\mu F \times 1.2V}{10\ \mu A} \times \left(1 - \frac{9V}{24V}\right) = 7.5\text{ msec} \tag{38}$$

8.2.2.15 Restart Capacitor C_{RES}

The restart capacitor determines restart delay time t_{RD} and hiccup mode off time t_{RES} (see Figure 26). t_{RD} must be greater than $t_{SS(MAX)}$. The minimum required value of C_{RES} can be calculated at the low input voltage as follows:

$$C_{RES(MIN)} = \frac{I_{RES} \times t_{SS(MAX)}}{V_{RES}} = \frac{30\ \mu A \times 7.5\text{ msec}}{1.2V} = 0.19\ \mu F \tag{39}$$

A standard value of 0.47 µF is selected for C_{RES}.

8.2.2.16 Low-Side Power Switch Q_L

Selection of the power N-channel MOSFET devices by breaking down the losses is one way to compare the relative efficiencies of different devices. Losses in the low-side N-channel MOSFET device can be separated into conduction loss and switching loss.

Low-side conduction loss is approximately calculated as follows:

$$P_{COND(LS)} = D \times I_{IN}^2 \times R_{DS\_ON(LS)} \times 1.3 = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \left(\frac{I_{OUT} \times V_{OUT}}{V_{IN}}\right)^2 \times R_{DS\_ON(LS)} \times 1.3\,[W] \tag{40}$$

Where, D is the duty cycle and the factor of 1.3 accounts for the increase in the N-channel MOSFET device on-resistance due to heating. Alternatively, the factor of 1.3 can be eliminated and the high temperature on-resistance of the N-channel MOSFET device can be estimated using the $R_{DS(ON)}$ vs temperature curves in the N-channel MOSFET datasheet.

Switching loss occurs during the brief transition period as the low-side N-channel MOSFET device turns on and off. During the transition period both current and voltage are present in the channel of the N-channel MOSFET device. The low-side switching loss is approximately calculated as follows:

$$P_{SW(LS)} = 0.5 \times V_{OUT} \times I_{IN} \times (t_R + t_F) \times f_{SW}\,[W] \tag{41}$$

t_R and t_F are the rise and fall times of the low-side N-channel MOSFET device. The rise and fall times are usually mentioned in the N-channel MOSFET data sheet or can be empirically observed with an oscilloscope.

An additional Schottky diode can be placed in parallel with the low-side N-channel MOSFET switch, with short connections to the source and drain in order to minimize negative voltage spikes at the SW node.

8.2.2.17 High-Side Power Switch Q_H and Additional Parallel Schottky Diode

Losses in the high-side N-channel MOSFET device can be separated into conduction loss, dead-time loss, and reverse recovery loss. Switching loss is calculated for the low-side N-channel MOSFET device only. Switching loss in the high-side N-channel MOSFET device is negligible because the body diode of the high-side N-channel MOSFET device turns on before and after the high-side N-channel MOSFET device switches.

High-side conduction loss is approximately calculated as follows:

$$P_{COND(HS)} = (1-D) \times I_{IN^2} \times R_{DS\_ON(HS)} \times 1.3 = \left(\frac{V_{IN}}{V_{OUT}}\right) \times \left(\frac{I_{OUT} \times V_{OUT}}{V_{IN}}\right)^2 \times R_{DS\_ON(HS)} \times 1.3 [W] \tag{42}$$

Dead-time loss is approximately calculated as follows:

$$P_{DT(HS)} = V_D \text{ x } I_{IN} \text{ x } (t_{DLH} + t_{DHL}) \text{ x } f_{SW} [W]$$

where

- V_D is the forward voltage drop of the high-side NMOS body diode. (43)

Reverse recovery characteristics of the high-side N-channel MOSFET switch strongly affect efficiency, especially when the output voltage is high. Small reverse recovery charge helps to increase the efficiency while also minimizes switching noise.

Reverse recovery loss is approximately calculated as follows:

$$P_{RR(HS)} = V_{OUT} \times Q_{RR} \times f_{SW} [W] \tag{44}$$

where

- Q_{RR} is the reverse recovery charge of the high-side N-channel MOSFET body diode. (45)

An additional Schottky diode can be placed in parallel with the high-side switch to improve efficiency. Usually, the power rating of this parallel Schottky diode can be less than the high-side switch's because the diode conducts only during dead-times. The power rating of the parallel diode should be equivalent or higher than high-side switch's if bypass operation is required, hiccup mode operation is required or any load exists before switching.

8.2.2.18 Snubber Components

A resistor-capacitor snubber network across the high-side N-channel MOSFET device reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and can couple noise to the output voltage. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. Start with a resistor value between 5 and 50 Ω. Increasing the value of the snubber capacitor results more damping, but this also results higher snubber losses. Select a minimum value for the snubber capacitor that provides adequate damping of the spikes on the switch waveform at heavy load. A snubber may not be necessary with an optimized layout.

8.2.2.19 Loop Compensation Components C_{COMP}, R_{COMP}, C_{HF}

R_{COMP}, C_{COMP} and C_{HF} configure the error amplifier gain and phase characteristics to produce a stable voltage loop. For a quick start, follow the following 4 steps:

1. Select f_{CROSS}

   Select the cross over frequency (f_{CROSS}) at one fourth of the RHP zero or one tenth of the switching frequency whichever is lower.

$$\frac{f_{SW}}{10} = 25\ \text{kHz} \tag{46}$$

$$\frac{f_{Z\_RHP}}{4} = \frac{R_{LOAD} \times (D')^2}{4 \times 2\pi \times L_{IN\_EQ}} = \frac{\frac{V_{OUT}}{I_{OUT}} \times (\frac{V_{IN}}{V_{OUT}})^2}{4 \times 2\pi \times L_{IN\_EQ}} = 5.3\ \text{kHz} \tag{47}$$

   5.3 kHz of the crossover frequency is selected between two. RHP zero at minimum input voltage should be considered if the input voltage range is wide.

2. Determine required R_{COMP}

   Knowing f_{CROSS}, R_{COMP} is calculated as follows:

$$R_{COMP} = f_{CROSS} \times \pi \times R_S \times R_{FB2} \times 10 \times C_{OUT} \times \frac{V_{OUT}}{V_{IN}} = 68.5\ \text{k}\Omega \tag{48}$$

   A standard value of 68.1 kΩ is selected for R_{COMP}

3. Determine C_{COMP} to cancel load pole. Place error amplifier zero at the twice of load pole frequency. Knowing R_{COMP}, C_{COMP} is calculated as follows:

$$C_{COMP} = \frac{R_{LOAD}\ \text{x}\ C_{OUT}}{4\ \text{x}\ R_{COMP}} = 20.2\text{nF} \tag{49}$$

   A standard value of 22 nF is selected for C_{COMP}

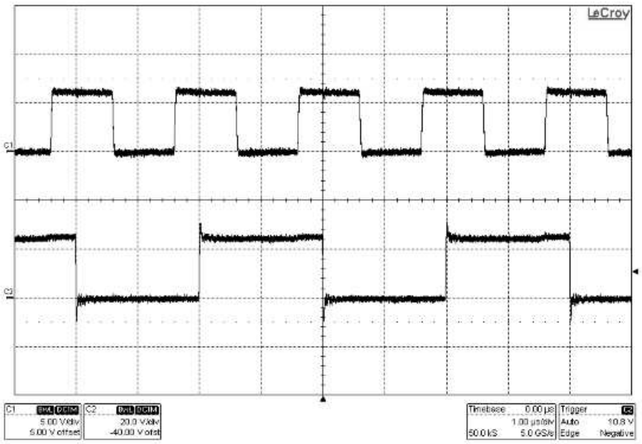
4. Determine C_{HF} to cancel ESR zero.

   Knowing R_{COMP}, R_{ESR} and C_{COMP}, C_{HF} is calculated as follows:

$$C_{HF} = \frac{R_{ESR} \times C_{OUT} \times C_{COMP}}{R_{COMP} \times C_{COMP} - R_{ESR} \times C_{OUT}} = 307\ \text{pF} \tag{50}$$

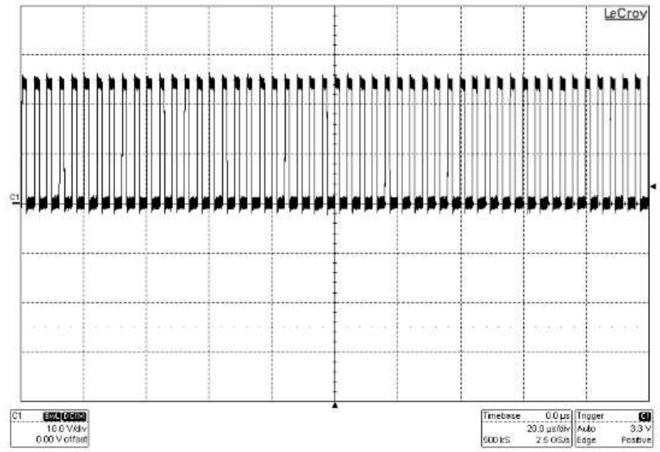
   A standard value of 330 pF is selected for C_{HF}.

8.2.3 Application Curves



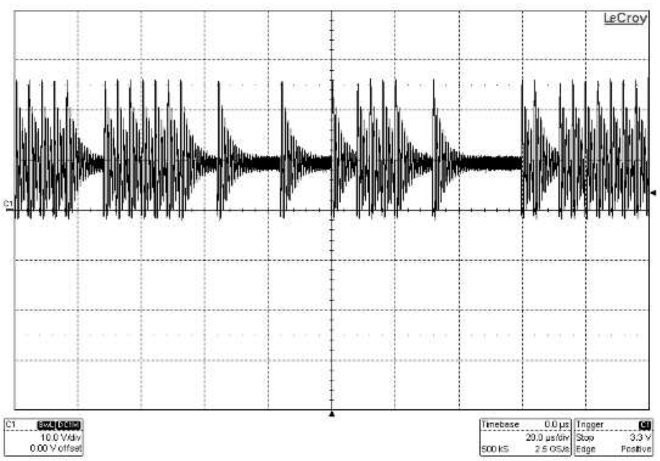
C1: F_{SYNC} C2: SW V_{SUPPLY} = 12 V, F_{SYNC} = 500 kHz

Figure 43. Clock Synchronization



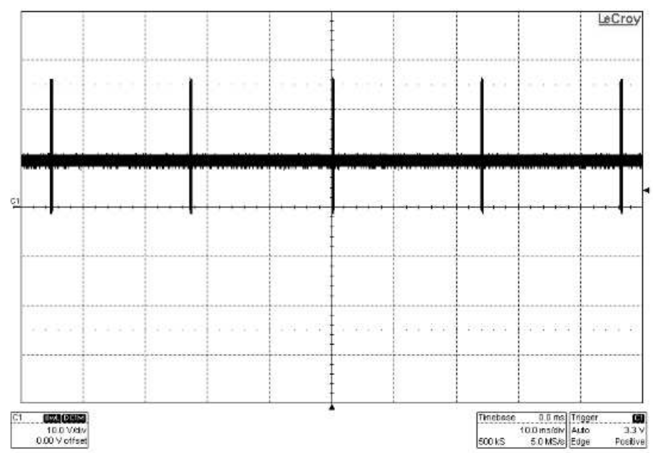
C1:SW V_{SUPPLY} = 12 V I_{LOAD} = 0 A

Figure 44. Forced PWM



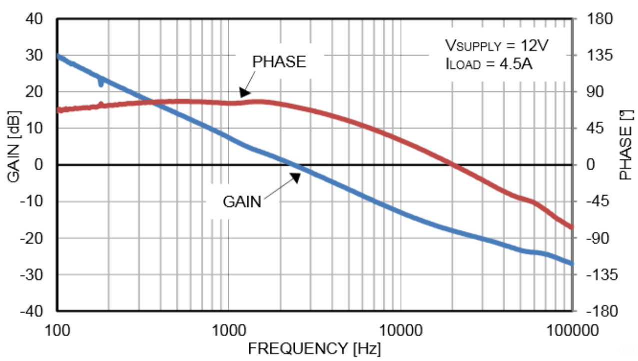
C1:SW V_{SUPPLY} = 12 V I_{LOAD} = 0 A

Figure 45. Pulse Skip



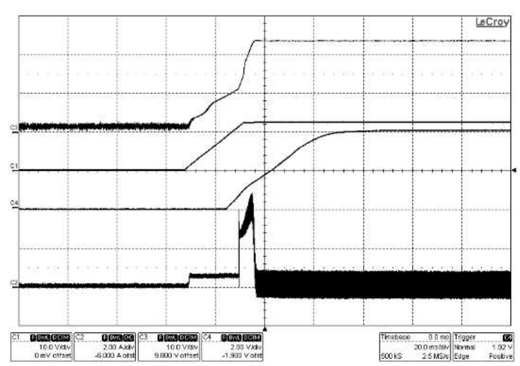
C1:SW V_{SUPPLY} = 12 V I_{LOAD} = 0 A

Figure 46. Skip Cycle



C1:SW V_{SUPPLY} = 12 V I_{LOAD} = 0 A

Figure 47. Loop Response



C1: V_{SUPPLY}, C2: Inductor current V_{SUPPLY} = 12 V
C3: V_{OUT}, C4: SS I_{LOAD} = 0 A

Figure 48. Start-Up

9 Power Supply Recommendations

The LM5122 is a power management device. The power supply for the device is any DC voltage source within the specified input range.

10 Layout

10.1 Layout Guidelines

In a boost regulator, the primary switching loop consists of the output capacitor and N-channel MOSFET power switches. Minimizing the area of this loop reduces the stray inductance and minimizes noise. Especially, placing high quality ceramic output capacitors as close to this loop earlier than bulk aluminum output capacitors minimizes output voltage ripple and ripple current of the aluminum capacitors.

In order to prevent a dv/dt induced turn-on of high-side switch, connect HO and SW to the gate and source of the high-side synchronous N-channel MOSFET switch through short and low inductance paths. In FPWM mode, the dv/dt induced turnon can occur on the low-side switch. Connect LO and PGND to the gate and source of the low-side N-channel MOSFET, through short and low inductance paths. All of the power ground connections must be connected to a single point. Also, all of the noise sensitive low power ground connections must be connected together near the AGND pin, and a single connection must be made to the single point PGND. CSP and CSN are high-impedance pins and noise sensitive. Route CSP and CSN traces together with kelvin connections to the current sense resistor as short as possible. If needed, place 100-pF ceramic filter capacitor close to the device. MODE pin is also high impedance and noise sensitive. If an external pullup or pulldown resistor is used at MODE pin, place the resistor close to the device. VCC, VIN and BST capacitor must be as physically close as possible to the device.

The LM5122 has an exposed thermal pad to aid power dissipation. Adding several vias under the exposed pad helps conduct heat away from the device. The junction to ambient thermal resistance varies with application. The most significant variables are the area of copper in the PC board, the number of vias under the exposed pad and the amount of forced air cooling. The integrity of the solder connection from the device exposed pad to the PC board is critical. Excessive voids greatly decrease the thermal dissipation capacity. The highest power dissipating components are the two power switches. Selecting N-channel MOSFET switches with exposed pads aids the power dissipation of these devices.

10.2 Layout Example

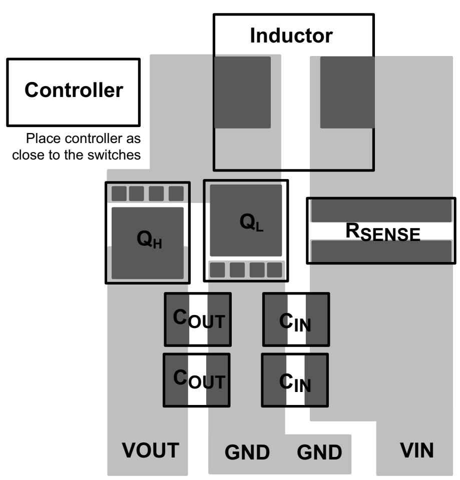


Figure 49. Power Path Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5122 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5122MH/NOPB	ACTIVE	HTSSOP	PWP	20	73	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM5122 MH	Samples
LM5122MHE/NOPB	ACTIVE	HTSSOP	PWP	20	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM5122 MH	Samples
LM5122MHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM5122 MH	Samples
LM5122ZPWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	LM5122Z MH	Samples
LM5122ZPWPT	ACTIVE	HTSSOP	PWP	24	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	LM5122Z MH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM5122 :

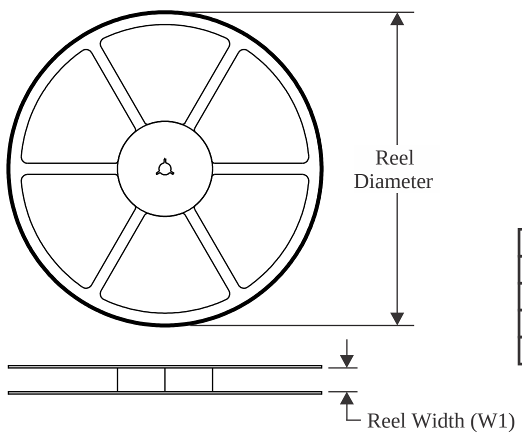
- Automotive: LM5122-Q1

NOTE: Qualified Version Definitions:

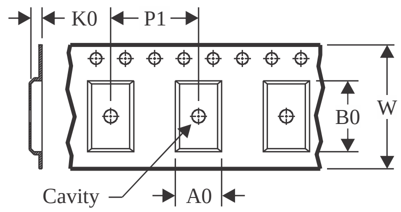
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

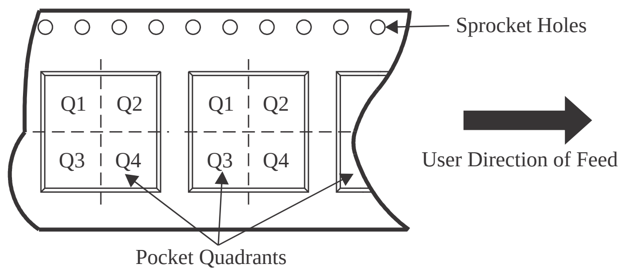


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

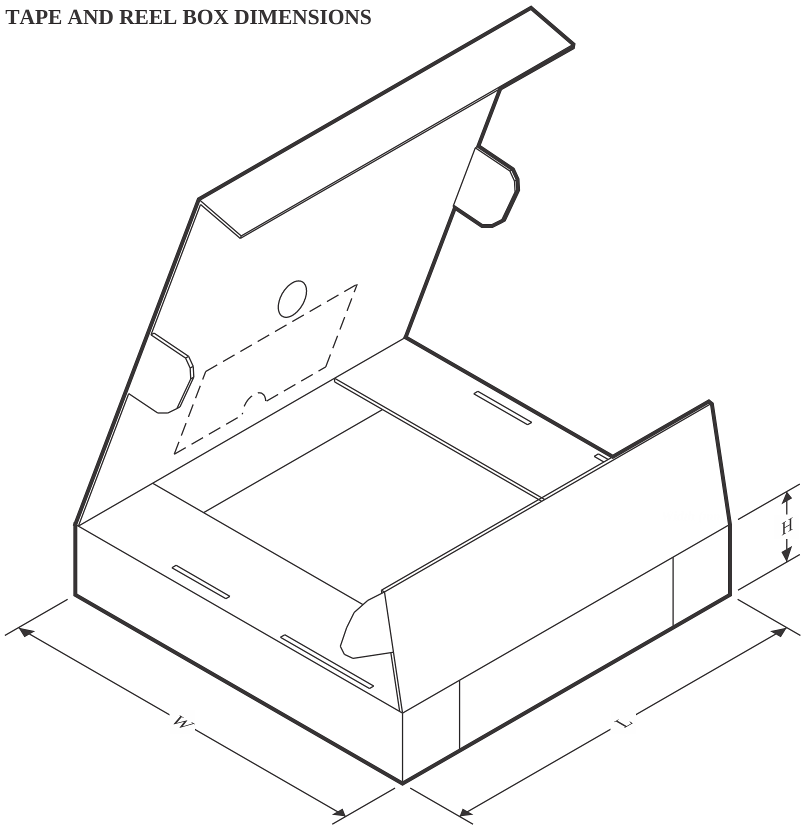
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5122MHE/NOPB	HTSSOP	PWP	20	250	178.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LM5122MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LM5122ZPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

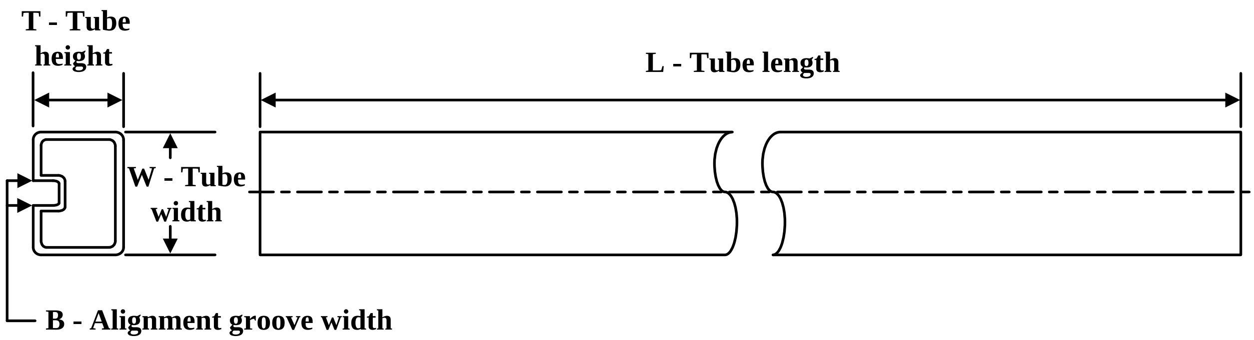
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5122MHE/NOPB	HTSSOP	PWP	20	250	208.0	191.0	35.0
LM5122MHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM5122ZPWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0

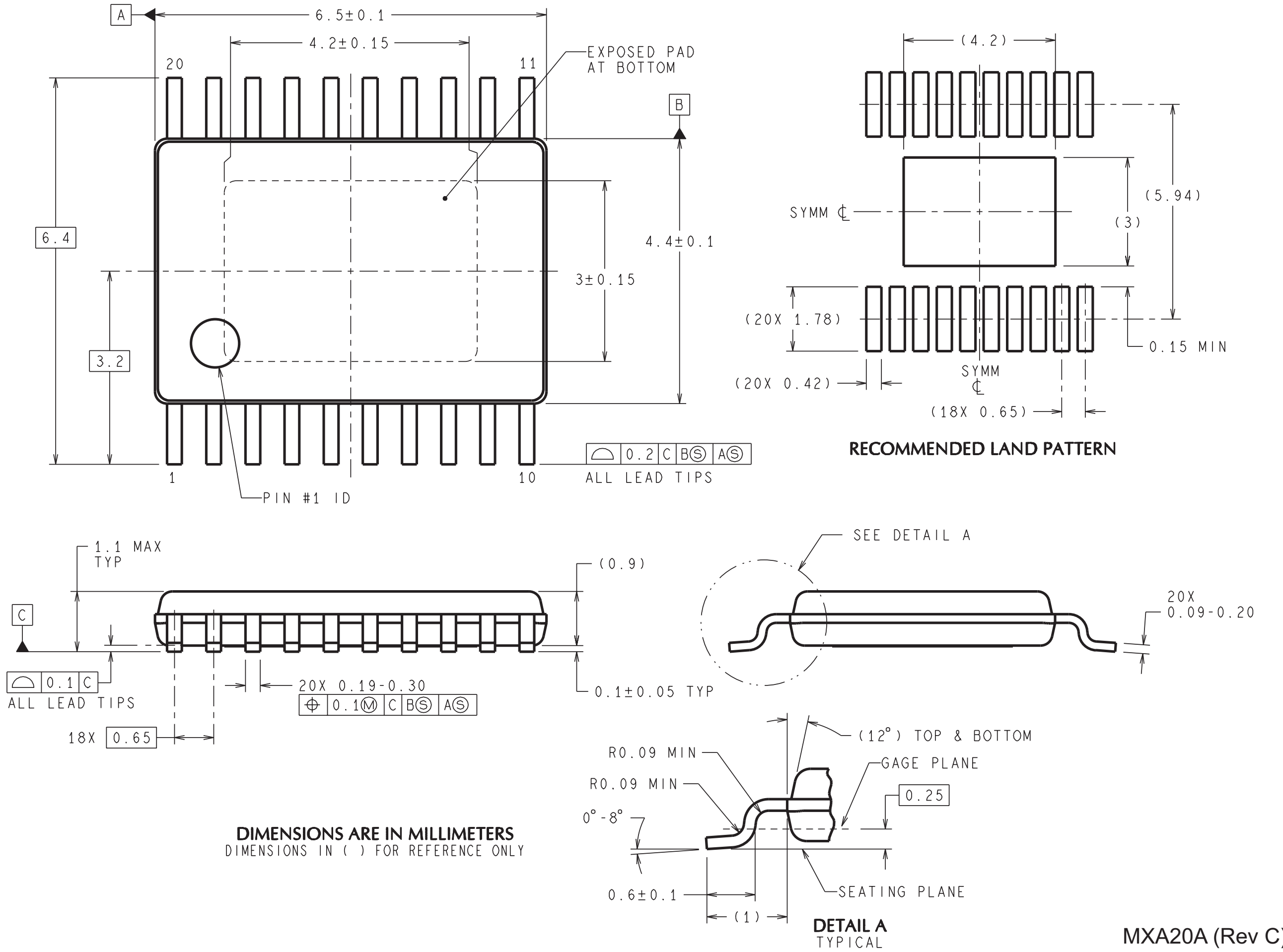
TUBE



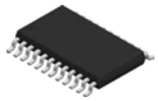
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5122MH/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06

PWP0020A



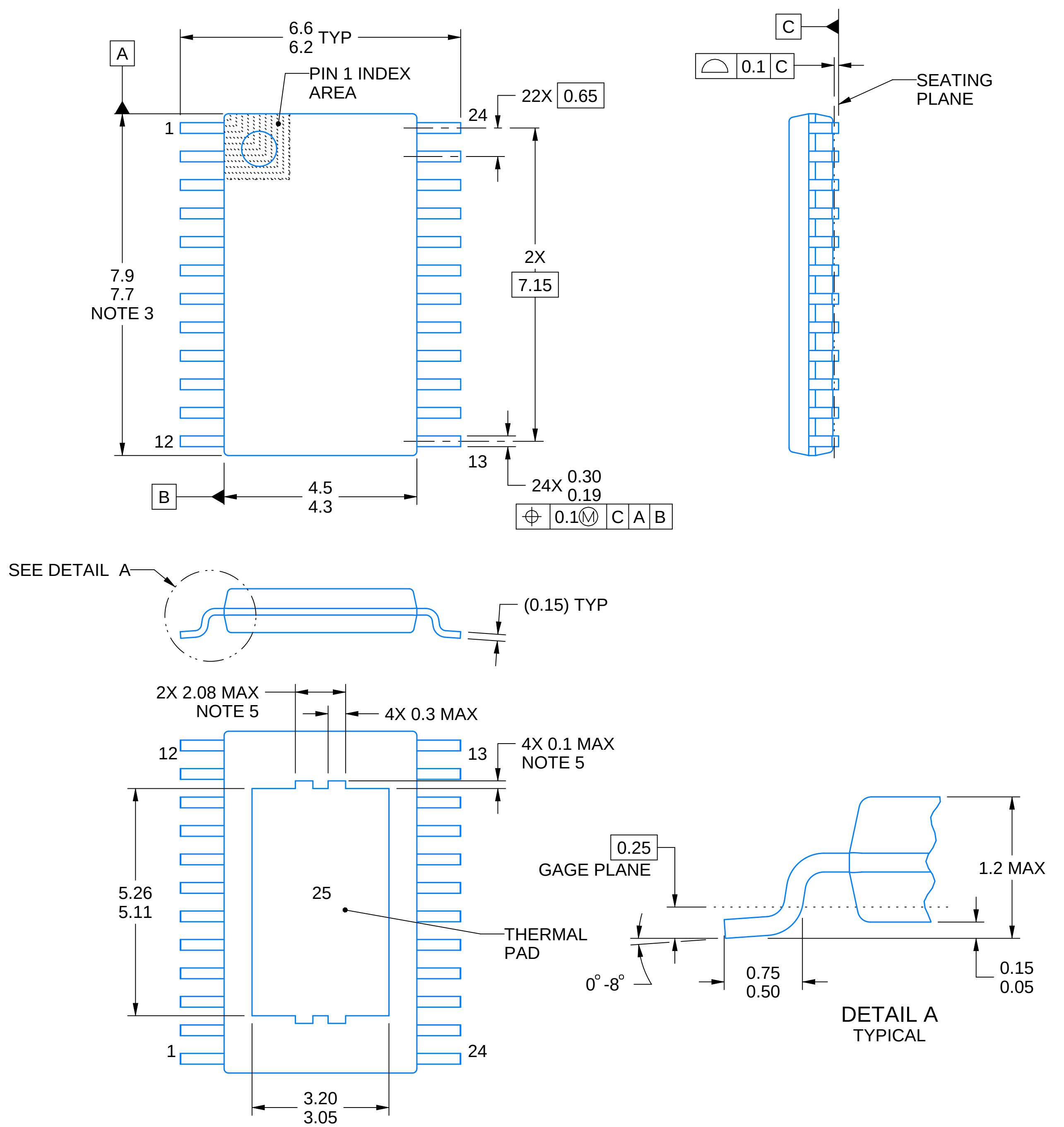
MXA20A (Rev C)



PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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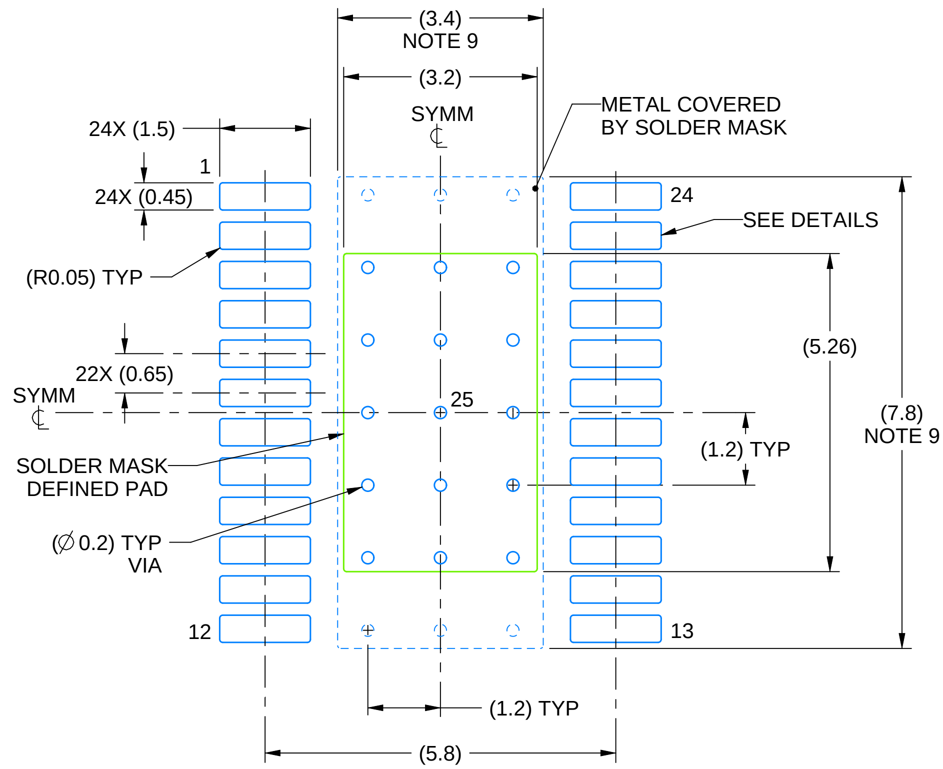
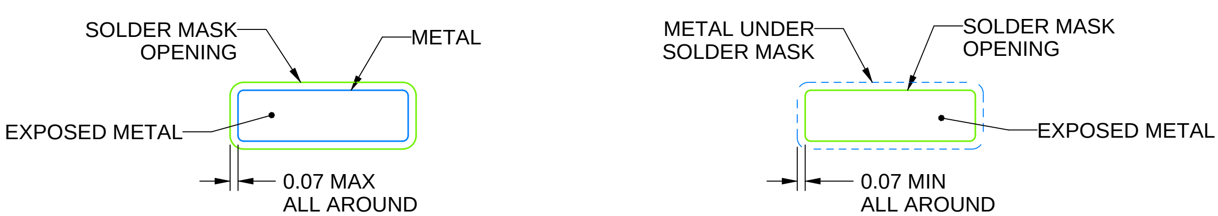
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



NON-SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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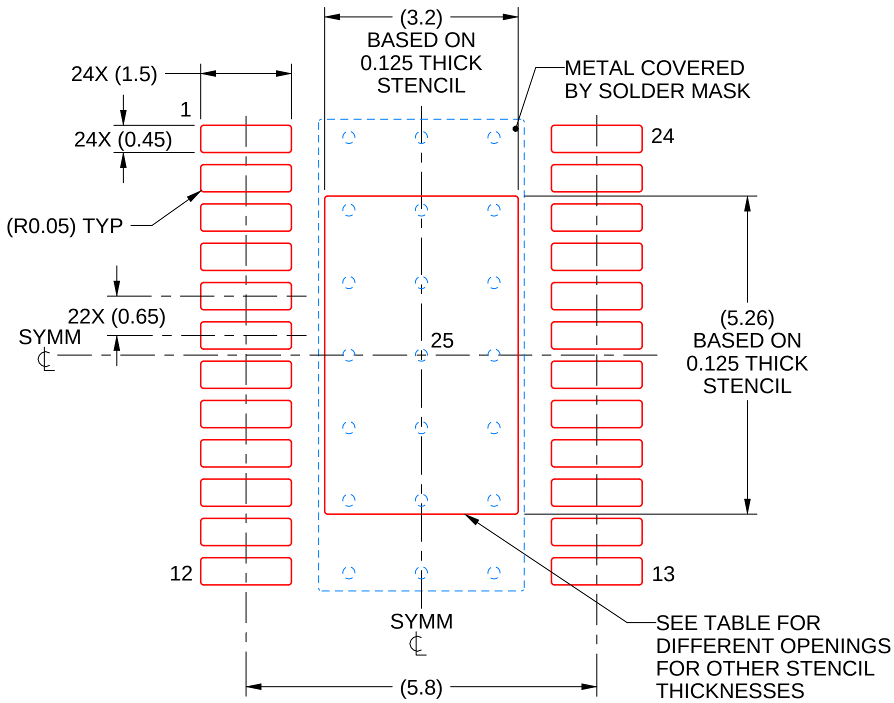
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.58 X 5.88
0.125	3.20 X 5.26 (SHOWN)
0.15	2.92 X 4.80
0.175	2.70 X 4.45

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265